ETM35E-10

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Application Manual

Real Time Clock Module

RX-8035SA/LC

SEIKO EPSON CORPORATION

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Contents

1. Overview 1
1.1. Features 1

2. Block Diagram 1

3. Pin Descriptions 2
3.1. Pin Layout 2
3.2. Pin Functions 2

4. Absolute Maximum Ratings 3

5. Recommended Operating Conditions 3

6. Frequency Characteristics 3

7. Electrical Characteristics 4
7.1. DC Electrical Characteristics 4
7.2. AC Electrical Characteristics(1) 5
7.3. AC Electrical Characteristics(2) 6

8. Usege 7
8.1. Overview of Functions 7
8.2 Automatic battery switch-over circuit. 8
8.3. Register table 10
8.4 Time stamp functions 18
8.4.1. EDFG bit 18
8.4.2 Time stamp registers. (BANK=1,address 0-6h) 18
8.4.3 EDCH1,EDCH2 Indication bit of event input terminal. 18
8.4.4EDFG bit of event detection function. 18
8.4.5 Event detection timing chart. 19
8.5 Clock Precision Adjustment Function 21
8.6 Periodic Interrupt Function 23
8.7 Alarm Interrupt Function 24
8.8. The various detection Functions 30
8.9 Overview of I2C-BUS 32

9. External Connection Example 36

10. External Dimensions / Marking Layout 37
10.1. External Dimensions 37
10.2. Marking Layout 37

11. Reference Data 38

12. Application notes 39

I²C-Bus Interface Real-time Clock Module

RX - 8035 SA / LC

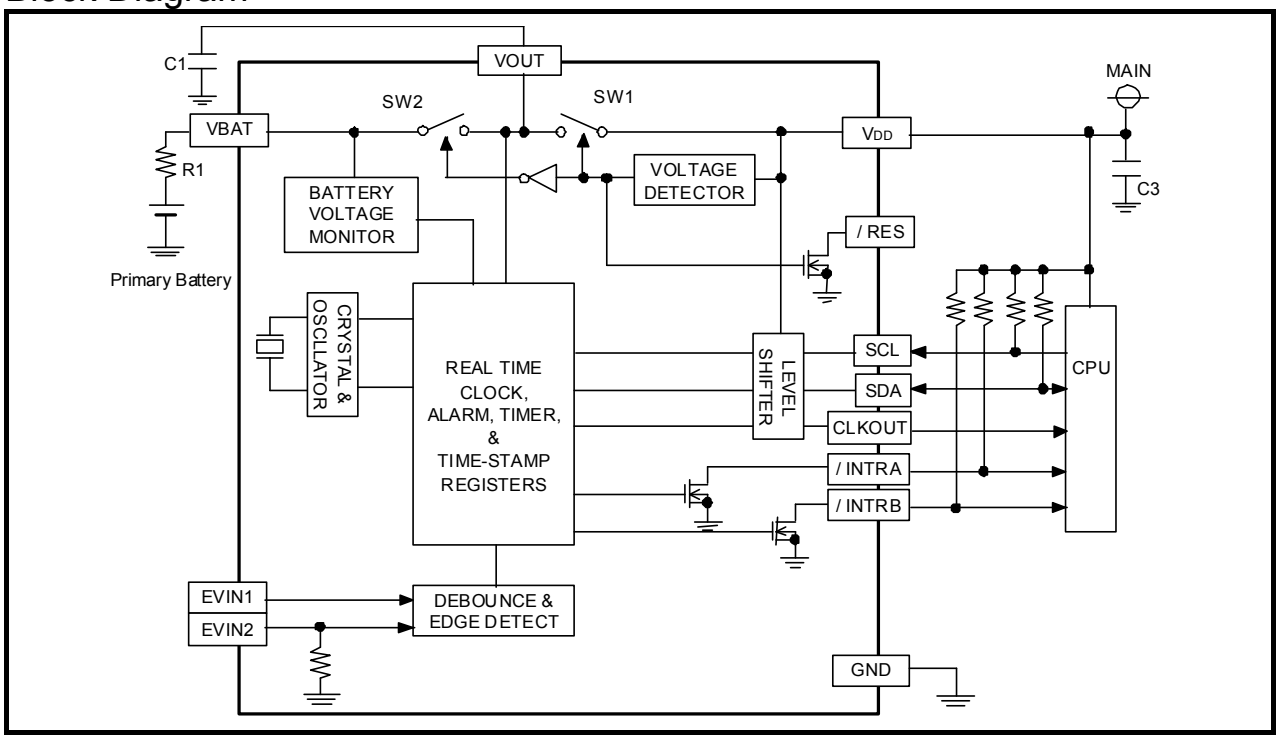
1. Overview

The RX-8035 is an I²C bus interface Real-time clock module which includes a 32.768kHz quartz oscillator that has been adjusted for high precision ± 5 ppm at +25°C.
This module provides time-stamp function and automatic battery switch-over circuit with low currents current consumption. And provides six types of interrupts, dual alarm function, oscillation stop detection, and power supply voltage monitoring. Since the internal oscillation circuit is driven by regulated voltage, 32.768kHz precision is stable and free of voltage fluctuation effects.
The RX-8035 is most suitable for power reduction, resource expansion of CPU, elimination of parts, improvement of tamper performance of a system in all electrical equipment.

1.1. Features

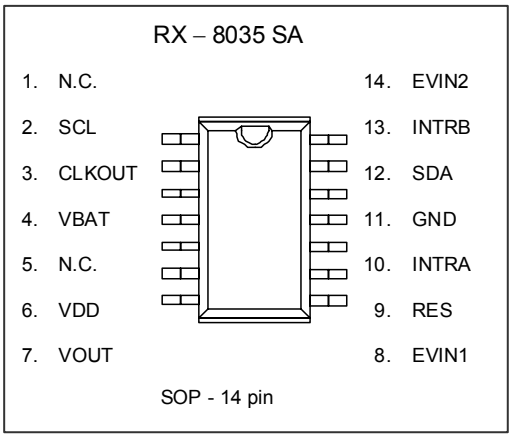
- Built-in 32.768kHz crystal unit : Frequency adjusted for high accuracy ($\pm 5 \times 10^{-6}$ at 25°C).
- Available automatic battery backup switch-over function.
- When internal power supply was switched from V_{DD} to battery, I²C-interface is inhibited, and Time data are protected automatically.
- Available time-stamp function and interrupt out to CPU by trigger input from two event input ports.
- Time-stamp function is available in supply from VDD or VBAT.
- Includes time (H/M/S) and calendar (YR/MO/WEEK/DATE/DAY) counter functions (BCD code)
- Selectable 12-hour mode or 24-hour clock mode.
- Auto calculation of leap years until 2099. (2100 is not leap year.)
- Dual alarm functions (Alarm_Wk: Day of week, Hour, Min. Alarm_Mo: Month, Day, Hour, Min)
- Oscillation stop detection function (used to determine reliability of internal data)
- Battery voltage monitoring function.
- Periodic interrupt function (Rate : Monthly, Hourly, every minute, every second, 0.5sec, OFF.)
- Built-in clock precision control logic
- 32.768kHz output. C-MOS
- Supports I²C-Bus's high speed mode (400 kHz)
- Wide clock voltage range: 1.0 V to 5.5 V
- Low current consumption: 350nA 3.0 V (Typ.) 8035SA

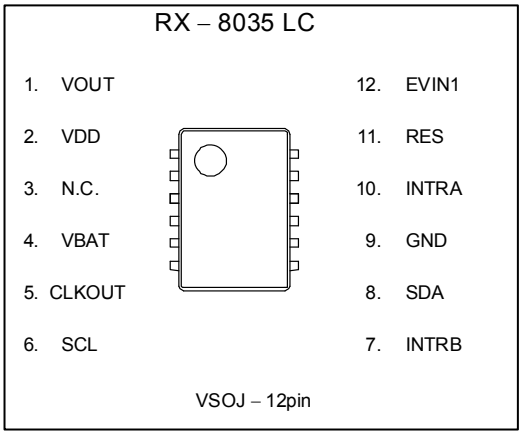
2. Block Diagram



3. Pin Descriptions

3.1. Pin Layout





3.2. Pin Functions

Signal name	I / O	Function
EVIN1	I	Event input terminal 1 for timestamp request. Built in de-bounce circuit. There is no built in resistor. A High level signal is a detection event.
EVIN2	I	Event input terminal 2 for timestamp request. Built in de-bounce circuit and pull-down resistor. A High level signal is a detection event.
RES	O	While monitoring V_{DD} input voltage, if the voltage is equal or lower than V_{D2B}, this output level is "L". When RES becomes "L", SW1 is open, and SW2 turns on. As a result, power is supplied from VBAT pin. When V_{DD} is equal to V_{B2D} or more, SW1 is closed, and SW2 is opened. After tDELAY passed, RES changes to Hi-Z status. It means system supply is stable. (SW1 and SW2: Please see Block diagram.)
SCL	I	Serial-clock input for I^2C communications. Up to 5.5 V can be used for this input, regardless of the power supply voltage. When V_{DD} is lower than V_{D2B}, I^2C interface is inactive.
SDA	I/O	Serial data inputs and outputs (N-ch open drain) for I^2C communications. Be sure to connect a suitable pull-up resistor relative to the signal line capacitance.
CLKOUT	O	32.768kHz CMOS output between GND to V_{DD}. It is always active.
INTRA	O	Outputs Alarm_Mo and event detection interrupts. N-ch open drain type.
INTRB	O	Outputs Alarm_Wk and periodic interrupts. N-ch open drain type.
V_{DD}	-	Input for main positive power supply. Be sure to connect a bypass capacitor rated at least 0.1 µF between V_{DD} and GND.
VBAT	-	Connect a battery or capacitor for backup power supply. Normally, power is supplied from V_{DD} to the IC. If V_{DD} level is equal or less than VD2B, power is supplied from this pin.
VOUT	O	Output of internal power source for outside devices. And the secondary battery can be connected. Be sure to connect a bypass capacitor rated at least 0.1 µF between VOUT and GND.
GND	-	For ground.
N.C.	-	Do not connect. Keep open.

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between V_{DD}, VOUT and GND.

4. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	V_{DD}	−0.3 to +6.5	V
	V_{BAT}	VBAT		
Input voltage	V_I	SCL, SDA, EVIN1,EVIN2	GND−0.3 to +6.5	V
Output voltage	V_{O1}	SDA, INTRA, INTRB	GND−0.3 to +6.5	V
	V_{O2}	CLKOUT, VOUT	GND−0.3 to V_{DD}+0.3	V
Output current	I_{OUT}	VOUT	20	mA
Operating Temperature	T_{OPR}		-40 to +85	°C
Storage temperature	T_{STG}		−55 to +125	°C

5. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{ACCESS}	V_{DD}	VD2B		5.5	V
Clock supply voltage	V_{CLK}	VBAT	1.00		5.5	V
Pull-up Voltage	V_{PUP}	SCL, SDA, INTRA, INTRB			5.5	V

6. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Frequency tolerance	Δ f / f	Ta = +25°C V_{DD} = 3.0 V	AA ; 5 ± 5 (*1) AC ; 0 ± 5(*1) B ; 5 ± 23(*2)	× 10^{-6}
Frequency/voltage characteristics	f / V	Ta = +25°C V_{DD} = 2 V to 5 V	± 1 Max.	× 10^{-6} / V
Frequency/temperature characteristics	Top	Ta = −20 °C to +70 °C, V_{DD} = 3.0 V; +25 °C reference	+10 / −120	× 10^{-6}
Detection voltage of oscillation stop.	VXSTP	XSTP = 1	1.0 Max.	V
Oscillation start time	t_{STA}	Ta = +25 °C V_{DD} = 2.0 V	1.0 Max.	s
Aging	fa	Ta = +25 °C V_{DD}=3.0 V; first year	± 5 Max.	× 10^{-6} / year

(*1)Equivalent to 13 seconds of monthly deviation.
(*2)Equivalent to 1 minute of monthly deviation.

7. Electrical Characteristics

7.1. DC Electrical Characteristics

* Unless otherwise specified, GND = 0 V, V_{DD} = 3 V, Ta = −40 °C to +85 °C

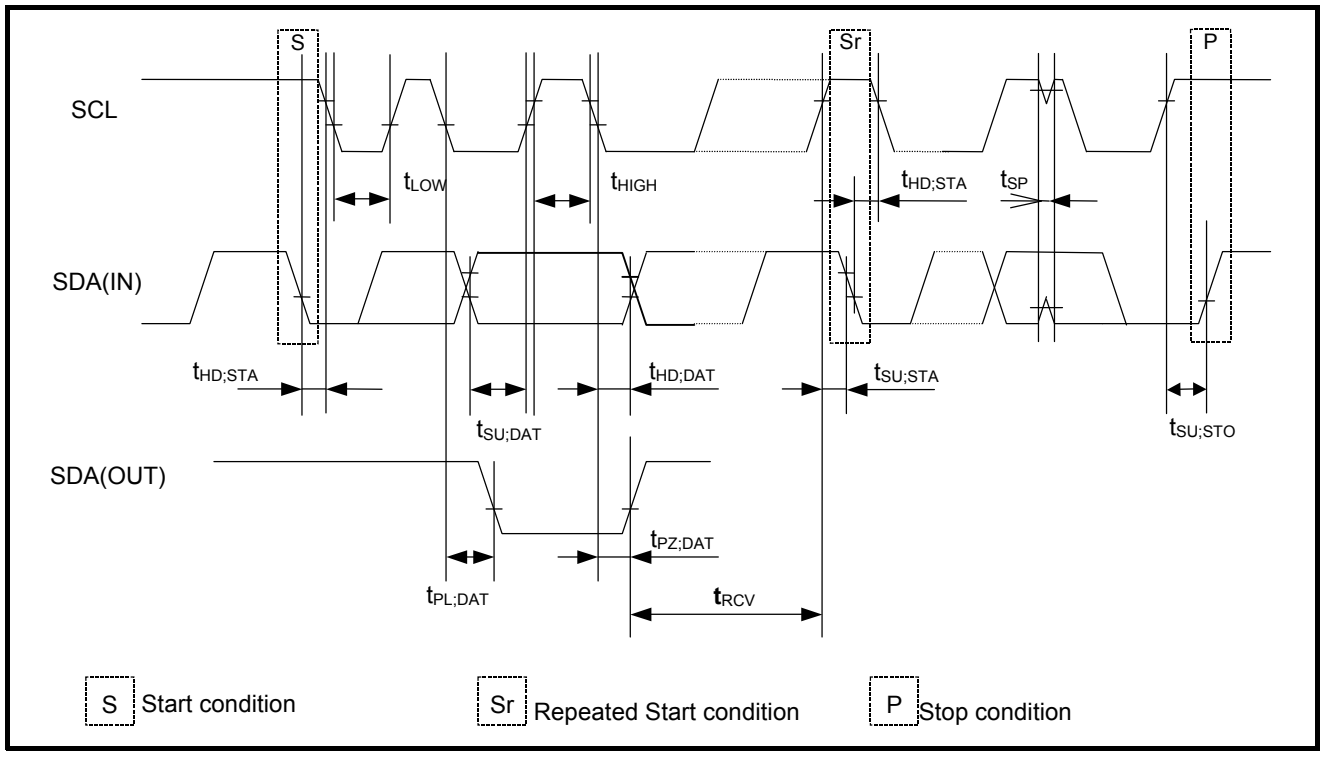
Symbol	Item	Pin name	Condition	Min.	Typ.	Max.	Unit
VIH1	"H" Input Voltage1	SCL, SDA	V_{DD} =1.5V to 5.5V	0.8x V_{DD}		5.5	V
VIL1	"L" Input Voltage1			-0.3		0.2x V_{DD}	
VIH2	"H" Input Voltage2	EVIN1, EVIN2	V_{DD}=1.0 to 5.5V	0.8x V_{DD}		5.5	V
VIL2	"L" Input Voltage2			-0.3		0.3	
IOH	"H" Output Current	CLKOUT	VOH=V_{DD}-0.5V			-0.5	mA
IOL1	"L" Output Current	CLKOUT	VOL=0.4V	0.5			mA
IOL2		/ INTRA / INTRB / RES		2.0			
IOL3		SDA		3.0			
IIL	Input Leakage Current	SCL	VI=5.5V or GND	-0.2		0.2	μA
IOZ	Output Off-state Current	/ INTRA, / INTRB, / RES, SDA	VO=5.5V or GND	-0.2		0.2	μA
RDN	Pull down resistor	EVIN2	built in.	40	120	400	kΩ
VD_{2B}	Detector Threshold Voltage. (falling edge of V_{DD})	V_{DD}	Ta=+25°C	2.328	2.40	2.472	V
V_{B2D}	Detector released Voltage. (rising edge of V_{DD})	V_{DD}	Ta=+25°C	2.396	2.52	2.544	V
$\frac{\Delta Detector}{\Delta Topt}$	Detector Threshold and Released Voltage Temperature coefficient	VD2B and VB2D of V_{DD}	Ta=-40 to +85°C		±100		$\times 10^{-6}$ / °C
VDET	VBAT Voltage Monitoring Voltage	VBAT	-	1.10	1.25	1.40	V
VDDOUT 1	VOUT output voltage 1	VOUT	Ta=+25°C, V_{DD}=3.0V (Iout=10mA)	V_{DD} -0.12	V_{DD} -0.03		V
VDDOUT 2	VOUT output voltage 2	VOUT	Ta=+25°C,V_{DD}=2.0V VBAT=3.0V (Iout=100μA)	VBAT -0.08	VBAT -0.03		V
IBAT1	RX-8035SA	VBAT	V_{DD}=0V, VBAT=3V SCL=SDA=0V EVIN1=EVIN2=GND CLKOUT = OPEN	-	350	1200	nA
	RX-8035LC				400		
IBATL	Leakage Current of VBAT pin	VBAT	V_{DD}=3.0V VBAT=0V or 5.5V SCL=SDA=0V CLKOUT = OPEN EVIN1=EVIN2=GND INTRA=INTRB = Hi-Z	-1.0	0.001	1.0	μA
IDD	V_{DD} current	V_{DD}		-	1.4	2.5	μA

7.2. AC Electrical Characteristics(1)

∗ Unless otherwise specified: GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = −40 °C to +85 °C
∗ Input conditions: V_{IH} = 0.8 × V_{DD}, V_{IL} = 0.2 × V_{DD}, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 ×V_{DD}, CL = 50 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}				400	kHz
SCL clock low time	t_{LOW}		1.3			µs
SCL clock high time	t_{HIGH}		0.6			µs
Start condition hold time	$t_{HD;STA}$		0.6			µs
Stop condition setup time	$t_{SU;STO}$		0.6			µs
Start condition setup time	$t_{SU;STA}$		0.6			µs
Recovery time from stop condition to start condition	t_{RCV}		62			µs
Data setup time	tSU:DAT		200			ns
Data hold time	tHDDAT		0			ns
SDA “L” stable time after falling of SCL	tPL;DAT				0.9	µs
SDA off stable time after falling of SCL	tPZ;DAT				0.9	µs
Rising time of SCL and SDA (input)	tR				300	ns
Falling time of SCL and SDA (input)	tF				300	ns
Spike width that can be removed with input filter	tSP				50	ns

note: RX-8035 supports 400kHz high-speed mode and 100kHz standard mode.



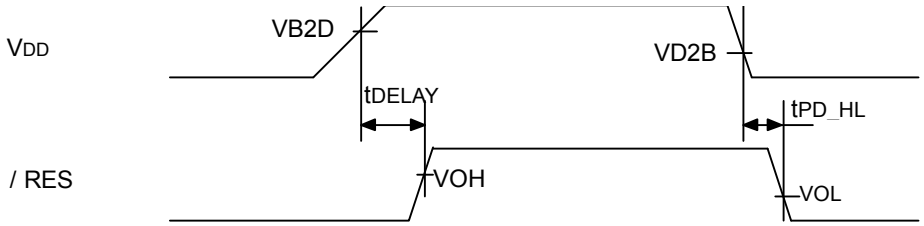
Caution: I^2C communication must be completed from START to STOP within 500ms.
If such communication requires over 1000ms, the I^2C bus interface is reset by the internal bus timeout function.

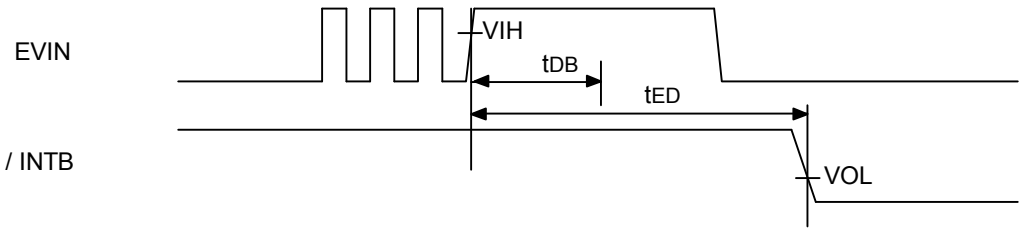
7.3. AC Electrical Characteristics(2)

∗ Unless otherwise specified: GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = −40 °C to +85 °C

∗ Input conditions: VIH = 0.8 × V_{DD}, VIL = 0.2 × V_{DD}, VOH = 0.8 × V_{DD}, VOL = 0.2 ×V_{DD}, CL = 50 pF

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
t_{DELAY} *1)	Output Delay Time of Voltage Detector.	$V_{DD} \geq V_{B2D}$	101	105	109	ms
t_{PD_HL}	Release Delay Time of Voltage Detector.	$V_{B2D} \geq V_{DD}$		15		µs
t_{DB} *1)	Debounce time of EVIN1 , EVIN2. Debounce time selects by DBSL bit.	DBSL=0	1992	1996	2000	ms
		DBSL=1	31	35	39	
t_{ED}	Event detection time		tDB +3.8	tDB + 7.8	tDB +11.8	ms





8. Usege

8.1. Overview of Functions

1) Clock and calendar functions
This function is used to set and read out month, date, day, hour, minute, and second.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099. (2100 is not leap year.)

2) Clock precision adjustment function
The clock precision can be adjusted forward or back in units of $\pm 3.05 \times 10^{-6}$. This function can be used to implement a higher precision clock function,

Note:
Only the clock precision can be adjusted. The adjustments have no effect on the 32.768kHz output from the CLKOUT pin.

3) Periodic interrupt function
In addition to the alarm function, Periodic interrupts can be output via the INTRA pin.
Select among five Periodic frequency settings: 2 Hz, 1 Hz, 1/60 Hz, hourly, or monthly.
Select among two output waveforms for periodic interrupts: an ordinary pulse waveform (2 Hz or 1 Hz) or a waveform (every second, minute, hour, or month) for CPU-level interrupts that can support CPU interrupts.
A polling function is also provided to enable monitoring of pin states via registers.

4) Alarm functions
This module is equipped with two alarm functions (Alarm Week and Alarm Month) that output interrupt signals to the host at preset times. The Alarm Week function can be used for day, hour, and minute-based alarm settings, and it outputs interrupt signals via the INTRB pin. Multiple day settings can be selected (such as Monday, Wednesday, Friday, Saturday, and Sunday). The Alarm Month function can be used for month, day, hour, and minute-based settings, and it outputs interrupt signals via the INTRA pin.
A polling function is also provided to enable checking of each alarm mode by the host.

5) Data reliability monitoring function.
When oscillation has stopped, XSTP bit is set to one by oscillation stop detector. When the battery voltage (VBAT terminal) drops than VDET voltage threshold value = 1.25 V (Typ.), VDET bit is set to one.
VDET detection is performed once per second in consideration of the module's low current consumption.
When initial power-on occur in this module, PON bit is set to one. Power-on-reset occurs in V_{DD} rise to VB2D from 0V and VBAT is 0V basically.

6) Interface with CPU
Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since neither SCL nor SDA includes a protective diode on the V_{DD} side, a data interface between hosts with differing supply voltages can still be implemented by adding pull-up resistors to the circuit board.
The SCL's maximum clock frequency is 400 kHz (when $V_{DD} \geq$ VB2D), which supports the I^2C bus's high-speed mode(400kHz) and standard mode(100kHz).

7) 32.768kHz clock output
The 32.768kHz clock (with precision equal to that of the built-in quartz oscillator) can be output via the FOUT pin.

Note:
The precision of this 32.768kHz clock output via the FOUT pin cannot be adjusted (even when using the clock precision adjustment function).
Clock output is driven by V_{DD} supply. Therefore, when V_{DD} voltage is 0V, clock output is 0V too.

8.2 Automatic battery switch-over circuit.

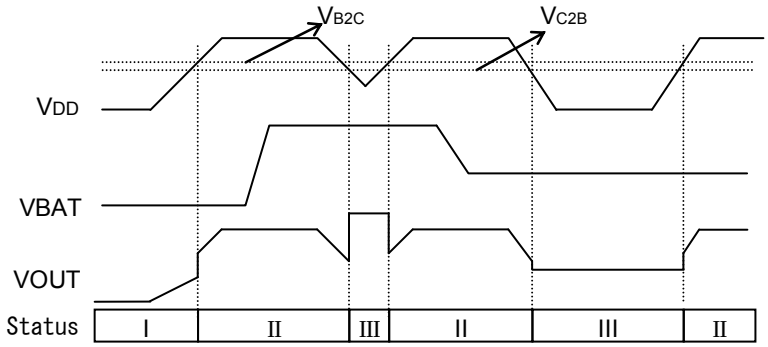
The RX-8035 has two power supply terminal (V_{DD} and VBAT) and one power output (VOUT). In case of V_{DD} voltage is less than VD2B, power is supplied from VBAT to keep real time clock function. Also I^2C interfaceis disabled to protect internal resistor value. When V_{DD} voltage rises to higher than VB2D, an internal power source is switched from VBAT to V_{DD}.

8.2.1 Example of RX-8035 setup procedure in completed product.

1: Attach battery for RX-8035.
2: Power supply from V_{DD}.
3: Sets the current date and time to RX-8035 from CPU.
4: Test the shipment inspection of a system.
5: Do not remove battery of RX-8035.
6: A power supply of a system is turned off.
7: A system is shipped for a customer.

Note
Either is good even if battery is set in RX-8035 first or even if VDD is given first.

8.2.2 Timing chart of V_{DD}, VBAT and VOUT.

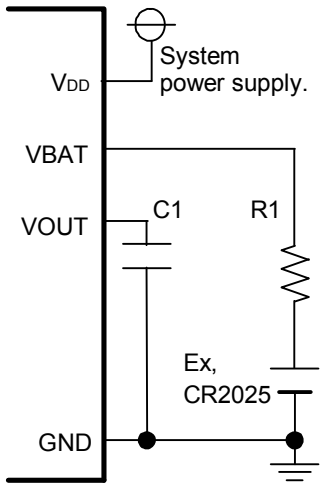


Explanation of chart.

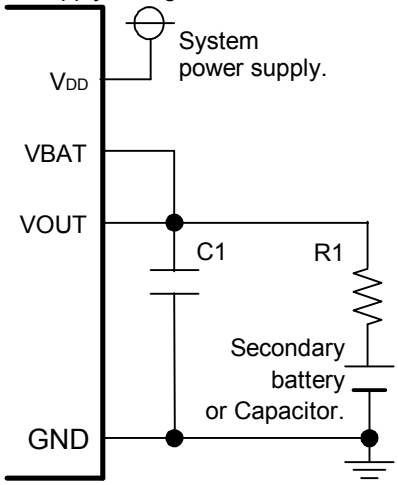
Status	Explanations
I	When power supplies from V_{DD} only initially. VOUT voltage follows about 1/2 V_{DD} voltage gradually before tern on internal circuits.
II	When V_{DD} voltage is above VB2D, VOUT outputs V_{DD} voltage.
III	When V_{DD} is less than VD2B, VOUT is equal with VBAT.

8.2.3 Examples of battery connections.

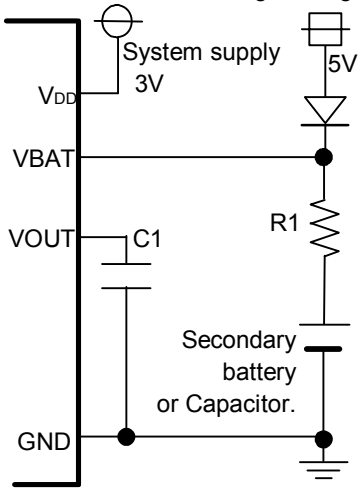
Case of primary battery connection.



Case of secondary battery connection.
And charge voltage = system supply voltage.

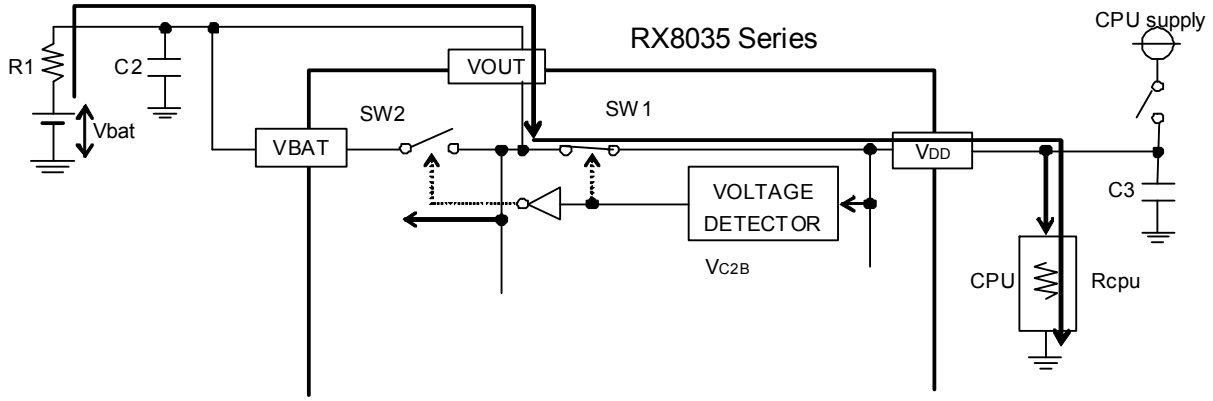


Case of secondary battery connection.
when the main power supply voltage is different from the charge voltage.



8.2.4 Note of battery switch-over circuit.

In case the RX-8035 with a rechargeable battery or a capacitor that charged from VOUT, the internal resistance of battery (R1) should be less than load resistance (Rcpu) as shown following figure.
Following figure shows just a timing to turn off V_{DD}, before turn off SW1. Current flow to Rcpu will be from a battery or capacitor via VOUT till SW1 off. If R1 is quite smaller than Rcpu, the input of voltage of voltage detector of V_{DD} is higher than VD2B. At this case SW1 is still on until a battery or a capacitor voltage meets VD2B then consume capacity of a battery or a capacitance.
Therefore R1 is limited by following formula.
$R1 > Rcpu \times (VBAT - (VD2B)) / (VB2D)$
And also sometimes R1 is limited by the specification of back up device. Please refer to specification of a battery or a capacitor.



8.3. Register table

BANK=0

Address	Function	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
0h	Seconds	-	S40	S20	S10	S8	S4	S2	S1
1h	Minutes	-	M40	M20	M10	M8	M4	M2	M1
2h	Hours	$\overline{12}$ /24	-	H20 P/$\overline{A}$	H10	H8	H4	H2	H1
3h	Day of week	-	-	-	-	-	W4	W2	W1
4h	Day of month	-	-	D20	D10	D8	D4	D2	D1
5h	Months	-	-	-	MO10	MO8	MO4	MO2	MO1
6h	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
7h	Digital Offset	TEST	F6	F5	F4	F3	F2	F1	F0
8h	Alarm_Wk ; Minute	*	WkM40	WkM20	WkM10	WkM8	WkM4	WkM2	WkM1
9h	Alarm_Wk ; Hour	*	*	WkH20 WkP/$\overline{A}$	WkH10	WkH8	WkH4	WkH2	WkH1
Ah	Alarm_Wk; Day of week.	*	WkW6	WkW5	WkW4	WkW3	WkW2	WkW1	WkW0
Bh	Alarm_Mo ; Minute	*	MoM40	MoM20	MoM10	MoM8	MoM4	MoM2	MoM1
Ch	Alarm_Mo ; Hour	*	*	MoH20 MoP/$\overline{A}$	MoH10	MoH8	MoH4	MoH2	MoH1
Dh	RAM	*	*	*	*	*	*	*	*
Eh	Control 1	WkALE	MoALE	DBSL	EDEN	TEST	CT2	CT1	CT0
Fh	Control 2	BANK TSFG	VDET	XSTP	PON	EDFG	CTFG	WkAFG	MoAFG

BANK=1

Address	Function	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
0h	Time-stamp Sec.	EDCH1	TS40	TS20	TS10	TS8	TS4	TS2	TS1
1h	Time-stamp Min	EDCH2	TM40	TM20	TM10	TM8	TM4	TM2	TM1
2h	Time-stamp Hour	-	-	TH20 TP/$\overline{A}$	TH10	TH8	TH4	TH2	TH1
3h	Time-stamp Day of Week	-	-	-	-	-	TW4	TW2	TW1
4h	Time-stamp Day of Month	-	-	TD20	TD10	TD8	TD4	TD2	TD1
5h	Time-stamp Month	-	-	-	TMO10	TMO8	TMO4	TMO2	TMO1
6h	Time-stamp Year	TY80	TY40	TY20	TY10	TY8	TY4	TY2	TY1
7h	Digital Offset	Same as BANK0							
8h	Reserved	-	-	-	-	-	-	-	-
9h		-	-	-	-	-	-	-	-
Ah		-	-	-	-	-	-	-	-
Bh	Alarm_Mo ; Day	DYE	*	MoD20	MoD10	MoD8	MoD4	MoD2	MoD1
Ch	Alarm_Mo ; Month	MOE	*	*	MoMO10	MoMO8	MoMO4	MoMO2	MoMO1
Dh	RAM	Same as BANK0							
Eh	Control 1	Same as BANK0							
Fh	Control 2	Same as BANK0							

∗1. The PON bit is a power-on reset flag bit.
The PON bit is set to "1" when a reset occurs, such as during the initial power-up or when recovering from a supply voltage drop. At the same time, all bits in the Alarm_Wk, Alarm_Mo, RAM, Digital Offset, Control 1 and Control 2 registers except for the PON, Vdet XSTP bits are reset to "0". And output of INTRA and INTRB are inhibited and Hi-Z.
Note: When PON = 1, all other register values are undefined, so be sure to perform a reset before using the module. Also, be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the time data is incorrect.

∗2. The TEST bits are used only testing in the factory. Clear all TEST bits to "0" always surely.

∗3. All bits marked with " – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

∗4. All bits marked with " ∗ " are read-write bits. As for these bits, set to 1 and clear are possible.

∗5. By the write-access, it is null and void to set 1 to PON, VDET,XSTP,.

8.3.1. Register map after power-on-reset.

●BANK=0

Address	Function	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
0h	seconds	–							
1h	minutes	–							
2h	houts		–						
3h	Day of week	–	–	–	–	–			
4h	Day of month	0	0						
5h	Month	0	0	0					
6h	Years								
7h	Digital offset	0	0	0	0	0	0	0	0
8h	Alarm_Wk ; Minute	0	0	0	0	0	0	0	0
9h	Alarm_Wk ; Hour	0	0	0	0	0	0	0	0
Ah	Alarm_Wk ; Day of Week	0	0	0	0	0	0	0	0
Bh	Alarm_Mo ; Minute	0	0	0	0	0	0	0	0
Ch	Alarm_Mo ; Hour	0	0	0	0	0	0	0	0
Dh	RAM	0	0	0	0	0	0	0	0
Eh	Control 1	0	0	0	0	0	0	0	0
Fh	Control 2	0	1	1	1	0	0	0	0

●BANK=1

Address	Function	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
0h	Time-stamp Sec.	0	0	0	0	0	0	0	0
1h	Time-stamp Min	0	0	0	0	0	0	0	0
2h	Time-stamp Hour	0	0	0	0	0	0	0	0
3h	Time-stamp Day of Week	0	0	0	0	0	0	0	0
4h	Time-stamp Day of Month	0	0	0	0	0	0	0	0
5h	Time-stamp Month	0	0	0	0	0	0	0	0
6h	Time-stamp Year	0	0	0	0	0	0	0	0
7h	Digital offset	Same as BANK0							
8h	Reserved	–	–	–	–	–	–	–	–
9h		–	–	–	–	–	–	–	–
Ah		–	–	–	–	–	–	–	–
Bh	Alarm_Mo ; Day	0	0	0	0	0	0	0	0
Ch	Alarm_Mo ; Month	0	0	0	0	0	0	0	0
Dh	RAM	Same as BANK0							
Eh	Control 1	Same as BANK0							
Fh	Control 2	Same as BANK0							

∗1. All bits marked with " – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

∗2. All bits marked with " ∗ " are read-write bits. As for these bits, set to 1 and clear are possible.

∗3. All bits marked with " / " are undefined bits after power-on-reset.

∗4. By the write-access, it is null and void to set 1 to PON, VDET, XSTP, MoAFG, WkAFG.

8.3.2. Time counter (Reg 0 to 2)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Seconds	–	S40	S20	S10	S8	S4	S2	S1
1	Minutes	–	M40	M20	M10	M8	M4	M2	M1
2	Hours	–	–	H20 P, /A	H10	H8	H4	H2	H1

- The time counter counts seconds, minutes, and hours.
- The data format is BCD format (except during 12-hour mode). For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the time counter.

1) Second counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Seconds	–	S40	S20	S10	S8	S4	S2	S1

- This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.
- When a value is written to the second counter, the internal counter is also reset to zero in less than one second.

2) Minute counter

Addres	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	Minutes	–	M40	M20	M10	M8	M4	M2	M1

- This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

3) Hour counter

Addres	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
2	Hours	$\overline{12}$ **/24**	–	H20 P , /A	H10	H8	H4	H2	H1

/12,24 bit

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

/12,24	Data	Description
Write / Read	0	12-hour clock ∗ Default
	1	24-hour clock

∗ Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

- The hour counter counts hours, and its clock mode differs according to the value of its /12,24 bit.
- During 24-hour clock operation, bit 5 functions as H20 (two-digit hour display). During 12-hour clock operation, bit 5 functions as an AM/PM indicator ("0" indicates AM and "1" indicates PM).

/12,24 bit	Description	Address 2 (Hours register) data [h] during 24-hour and 12-hour clock operation modes
0	12-hour clock	
1	24-hour clock	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	12 (AM 12)	12	32 (PM 12)
01	01 (AM 01)	13	21 (PM 01)
02	02 (AM 02)	14	22 (PM 02)
03	03 (AM 03)	15	23 (PM 03)
04	04 (AM 04)	16	24 (PM 04)
05	05 (AM 05)	17	25 (PM 05)
06	06 (AM 06)	18	26 (PM 06)
07	07 (AM 07)	19	27 (PM 07)
08	08 (AM 08)	20	28 (PM 08)
09	09 (AM 09)	21	29 (PM 09)
10	10 (AM 10)	22	30 (PM 10)
11	11 (AM 11)	23	31 (PM 11)

8.3.3. Day counter (Reg 3)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3	Day of Week	–	–	–	–	–	W4	W2	W1

- The day counter is a divide-by-7 counter that counts from 00 to 01 and up 06 before starting again from 01.
- The correspondence between days and count values is shown below.

Days	W4	W2	W1	Day	Remark
Write / Read	0	0	0	Sunday	00 h
	0	0	1	Monday	01 h
	0	1	0	Tuesday	02 h
	0	1	1	Wednesday	03 h
	1	0	0	Thursday	04 h
	1	0	1	Friday	05 h
	1	1	0	Saturday	06 h
Write prohibit	1	1	1	–	Do not enter a setting for this bit.

Weekday layout is one of example.

8.3.4. Calendar counter (Reg 4 to 6)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	Day of Month	–	–	D20	D10	D8	D4	D2	D1
5	Months	–	–	–	MO10	MO8	MO4	MO2	MO1
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

∗ Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

1) Date counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	Days	–	–	D20	D10	D8	D4	D2	D1

- The updating of dates by the date counter varies according to the month setting.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96).

Days	Month	Date update pattern
Write / Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 to 30, 31, 01…
	4, 6, 9, or 11	01, 02, 03 to 30, 01, 02…
	February in leap year	01, 02, 03 to 28, 29, 01…
	February in normal year	01, 02, 03 to 28, 01, 02…

2) Month counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
5	Months	–	–	–	MO10	MO8	MO4	MO2	MO1

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

3) Year counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.

∗ In any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.), the dates in February are counted from 01, 02, 03 and up to 29 before starting again at 01.

8.3.5. Clock precision adjustment register (Reg 7)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	Digital Offset (Default)	TEST (0)	F6 (0)	F5 (0)	F4 (0)	F3 (0)	F2 (0)	F1 (0)	F0 (0)

- The binary encoded settings in the seven bits from F6 to F0 are used to set the precision of the clock generated from the 32.768kHz internal oscillator up to $\pm 189 \times 10^{-6}$ in the forward (ahead) or reverse (behind) direction, in units of $\pm 3.05 \times 10^{-6}$. (Only the clock precision can be adjusted. The 32.768kHz output from the FOUT pin is not affected.)
- When not using this function, be sure to set "0" for bits F6 to F0.
- Always, clear TEST bits to "0" surely.

∗ For details, see "9.4. Clock Precision Adjustment Function".

8.3.6. Alarm_Wk register (Reg 8 to A)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	Alarm_Wk ; Minute	–	WkM40	WkM20	WkM10	WkM8	WkM4	WkM2	WkM1
9	Alarm_Wk ; Hour	–	–	WkH20 WkP , /A	WkH10	WkH8	WkH4	WkH2	WkH1
A	Alarm_Wk ; Day	–	WkW6	WkW5	WkW4	WkW3	WkW2	WkW1	WkW0

- The Alarm_Wk function is used, along with the WkALE and WkAFG bits, to set alarms for specified day, hour, and minute values.
- When the Alarm_Wk setting matches the current time, INTRB pin is set to "L" and the WkALE bit is set to "1".
  Note: If the current date/time is used as the Alarm_Wk setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_Wk ; Hours" register's bit 5 (WkH20, WkP, /A) functions as WkH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.
- When the Alarm_Wk function's day values (WkW6 to WkW0) are all "0" Alarm_Wk does not occur.

8.3.7. Alarm_ Month register (Reg B and C)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Alarm_Mo ; Minute	–	MoM40	MoM20	MoM10	MoM8	MoM4	MoM2	MoM1
C	Alarm_Mo ; Hour	–	–	MoH20 MoP , /A	MoH10	MoH8	MoH4	MoH2	MoH1

- The Alarm Month function is used, along with the MoALE and MoAFG bits, to set alarms for specified hour and minute values.
- When the Alarm_Month setting matches the current time, INTRA pin is set to "L" and the MoALE bit is set to "1".
  Note: If the current time is used as the Alarm_Mo setting, the alarm will not occur until the counter counts up to the current time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_Mo ; Hours" register's bit 5 (MoH20, MoP, /A) functions as MoH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.

8.3.8. RAM register (Reg D)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	User RAM	*	*	*	*	*	*	*	*

- These bits, set to 1 and clear are possible.

8.3.9. Control register 1 (Reg E)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Control 1 (Default)	WkALE (0)	MoALE (0)	DBSL (0)	EDEN (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)

∗) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.

1) WkALE bit

This bit is used to set up the Alarm Wk function (to generate alarms matching day, hour, or minute settings).

WkALE	Data	Description
Write / Read	0	Alarm_Wk, match comparison operation invalid ∗ Default
	1	Alarm_Wk, match comparison operation valid (INTRB = "L" when match occurs)

∗ For details, see "9.6.6. Alarm Wk Function".

2) MoALE bit

This bit is used to set up the Alarm Mo function (to generate alarms matching hour or minute settings).

MoALE	Data	Description
Write / Read	0	Alarm_Mo, match comparison operation invalid ∗ Default
	1	Alarm_Mo, match comparison operation valid (INTRA = "L" when match occurs)

∗ For details, see "9.6.5. Alarm Mo Function".

3) DBSL bit

This bit is used to select de-bounce time in EVIN input.

DBSL	Data	Description
Write / Read	0	De-bounce time are set up to 1996ms. (Typ.) ∗ Default
	1	De-bounce time are set up to 35ms. (Typ.)

4) EDEN bit

This bit enables Event Detection and Timestamp function.

EDEN	Data	Description
Write / Read	0	Event detection are stops, and BANK-1 data are cleared. Address0,1,2,4,5,6 of Bank1 and EDFG of address F too. ∗ Default
	1	Enables event detection and timestamp.

5) TEST bit

This bit is used by the manufacturer for testing. Always, clear this bit to "0" surely.
Be careful to avoid writing a "1" to this bit when writing to other bits.

TEST	Data	Description
Write / Read	0	Normal operation mode ∗ Default
	1	Setting prohibited (Factory test mode)

6) CT2, CT1, and CT0 bits

These bits are used to set up the operation of the periodic interrupt function that uses the INTRB pin.

CT2	CT1	CT0	INTRB pin's output setting		
			Waveform mode	Cycle/Fall timing	
0	0	0	–	INTRB = Hi-Z (= OFF)	∗ Default
0	0	1	–	INTRB = Fixed low	
0	1	0	Pulse mode ∗1)	2 Hz	(50% duty)
0	1	1	Pulse mode ∗1)	1 Hz	(50% duty)
1	0	0	Level mode ∗2)	Once per second	(Synchronous with per-second count-up)
1	0	1	Level mode ∗2)	Once per minute	(Occurs when seconds reach ":00")
1	1	0	Level mode ∗2)	Once per hour	(Occurs when minutes and seconds reach "00:00")
1	1	1	Level mode ∗2)	Once per month	(Occurs at 00:00:00 on first day of month)

∗ For details, see "9.5.. Periodic Interrupt".

8.3.10. Control register 2 (Reg F)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control 2	BANK TSFG	VDET	XSTP	PON	EDFG	CTFG	WkAFG	MoAFG
	(Default)	(0)	(0)	(–)	(1)	(0)	(0)	(0)	(0)

1)The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
2)" – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

1) BANK bit
This bit uses switch to Bank0 or Bank1.

2) TSFG bit
This bit indicate reliability of the timestamp data.
When timestamp event occurs, if XSTP and VDET was "0" both, then TSFG is set to "1".
Or if one of XSTP or VDET are set, then TSFG are cleared to "0".

BANK TSFG	Data	Description
Write (BANK)	0	Access is possible to a register of BANK0. Time and calendar. ∗ Default
	1	Access is possible to a register of BANK1. Time stamp data.
Read (TSFG)	0	Time stamp data are invalidly. ∗ Default When clears EDEN bit, TSFG bit clears too.
	1	Time stamp data are validly.

3) VDET bit
VDET shows that the inside voltage was less than VDET

VDET	Data	Description
Write	0	Clears the VDET bit to zero, restarts the VBAT drop detection operation and sets up for next VBAT drop detection operation ∗ Default
	1	Can not write 1.
Read	0	VBAT drop was not detected ∗ Default
	1	VBAT drop was detected (result is that bit value is held until cleared to zero)

∗ For details, see "9.7. Detection Functions".

4) XSTP bit
XSTP must be cleared to zero before it is used.
When it was detected a vibration stop, XSTP is set to "1". "0" shows that there is not a stop of an oscillation.
If detect oscillation stop, XSTP set to "1". (Note: The logic of this bit is reverse of RX-8025.)

XSTP	Data	Description
Write	0	Starts the oscillation stop detection function.
	1	Can not write 1.
Read	0	Oscillation stop was not detected
	1	Oscillation stop was detected ∗ Default (result is that bit value is held until a "0" is written)

4) PON bit
This bit indicates the power-on reset detection function's detection results.
The PON bit is set (= 1) when the internal power-on reset function operates.

PON	Data	Description
Write	0	Clears the PON bit to zero and sets up next detection operation
	1	Can not write 1.
Read	0	Power-on reset was not detected
	1	Power-on reset was detected. ∗ Default (result is that bit value is held until cleared to zero)

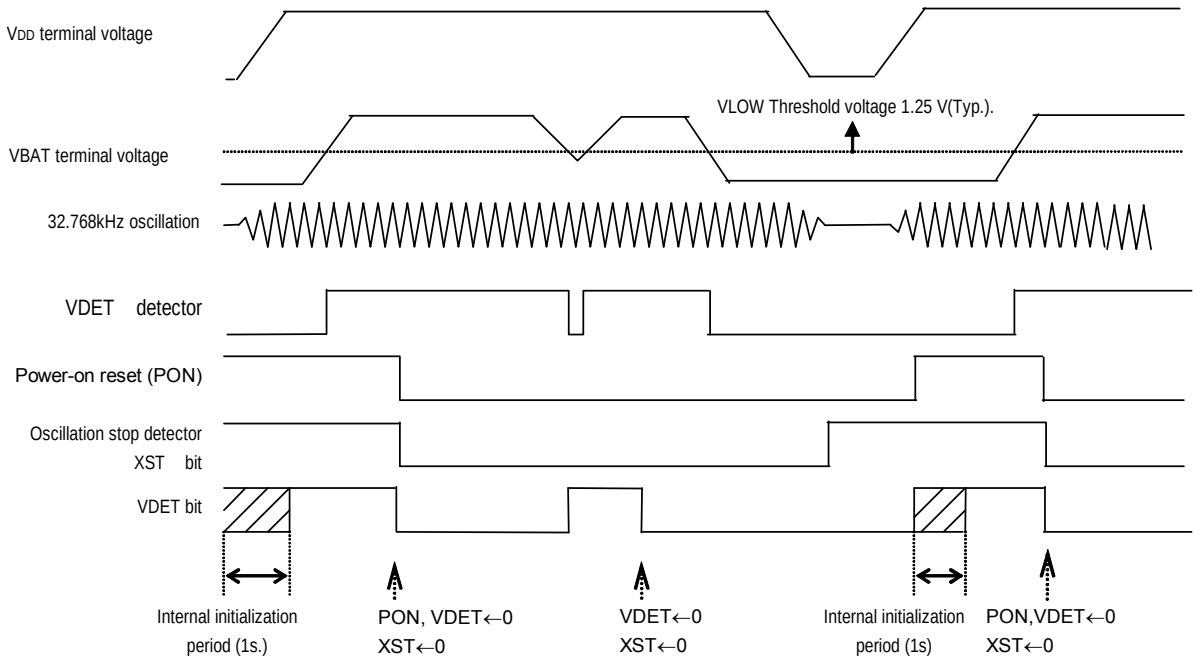
∗ When PON = "1" all bits in the Clock Precision Adjustment register and in the Control 1 and Control 2 registers (except for the PON, VDET and XSTP bits) are reset to "0". This also causes output from INTRA and INTRB pin to be stopped (= Hi-Z).
VDD should rise from less than 0.2V so that Power-On-Reset occurs.
VBAT need less than 0.2V too.

8.3.11. Diagnosis of status based on detection results

The status of power supplies and reliability of time and calendar can be confirmed by reading the detection results indicated by PON bit, XSTP bit and VDET bit.

The following are status diagnosis based on various combinations of detection results.

Address F h Control 2 Register			Diagnosis of status	
bit 4	bit 5	bit 6	Status of power supply and oscillation circuit	Status of clock and backup
PON	XSTP	VDET		
0	1	0	• Supply voltage was normal. But oscillation has stopped.	• Clock abnormality has occurred → Initialization is required ∗ Clock has stopped temporarily, possibly due to mechanical clash, etc.
0	1	1	• Supply voltage has dropped and oscillation has stopped.	• Clock abnormality has occurred → Initialization is required。 ∗ Clock has stopped, maybe due to drop in backup power supply.
0	0	0	• Normal status.	• Normal status.
0	0	1	• Supply voltage has dropped but oscillation continues.	• Maybe initialization is unnecessary. But, exchange of a battery will be necessary.
1	1	X	• Supply voltage has dropped to 0 V.	• Initialization is required regardless of the clock status and whether or not a voltage drop has occurred. Initialization is required.
1	0	X	• Power supply flickering is likely.	



8.4 Time stamp functions.

8.4.1. EDFG bit

When an event signal valid was detected, EDFG is set. An event terminal detected first is recorded in EDCH1, EDCH2, after EDEN was set.When it was detected at the same time by two terminals, both bits are set.

EDFG	status
0	Event detection does not yet occur.
1	Event detected.

(Default)

Note: "1" is not written in EDFG. Only zero clear is possible.

8.4.2 Time stamp registers. (BANK=1,address 0-6h)

Adrs	Function	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
0h	Time-stamp Sec.	EDCH1	TS40	TS20	TS10	TS8	TS4	TS2	TS1
1h	Time-stamp Min	EDCH2	TM40	TM20	TM10	TM8	TM4	TM2	TM1
2h	Time-stamp Hour	-	-	TH20 TP/ $\overline{A}$	TH10	TH8	TH4	TH2	TH1
3h	Time-stamp Day of Week	-	-	-	-	-	TW4	TW2	TW1
4h	Time-stamp Day of Month	-	-	TD20	TD10	TD8	TD4	TD2	TD1
5h	Time-stamp Month	-	-	-	TMO10	TMO8	TMO4	TMO2	TMO1
6h	Time-stamp Year	TY80	TY40	TY20	TY10	TY8	TY4	TY2	TY1

・All time stamp register are read only. Either date and time when an event was input first of an EVIN1 terminal and a RVIN2 terminal are recorded. The next event is not recorded unless EDEN is set to 1 from 0 again. When EDEN bit is cleared, all time stamp registers are cleared by zero. Therefore, time stamp data must be read before clearing an EDEN bit surely.

8.4.3 EDCH1,EDCH2 Indication bit of event input terminal.

EDCH2	EDCH1	Result.
0	0	Events is not detected. (Default)
0	1	Event was detected in EVIN1 terminal.
1	0	Event was detected in EVIN2 terminal.
1	1	Two event was detected in EVIN1 and EVIN2 terminals same time.

Note: When two signals were input between 7.8ms(Max.), it is judged to be the input of the same time.

8.4.4EDFG bit of event detection function.

EDFG	result.
0	Event input is not detected.
1	Event input is detected.

(Default 値)

When EDEN bit is 1, event input is detected in High from Low of EVIN terminal (tDB) time later.

After 7.8ms, EDFG bit is set to and INT terminal asserted to Low.

Detected event terminal is memorized in EDCH1,EDCH2.

When detected EVIN1; EDCH1=1,

When detected EVIN2; EDCH2=1,

When during time of tDB, EVIN1 and EVIN2 kept high level, then both EDCH1 and EDCH2 are set to 1 .

This time is recorded by a time stamp register.

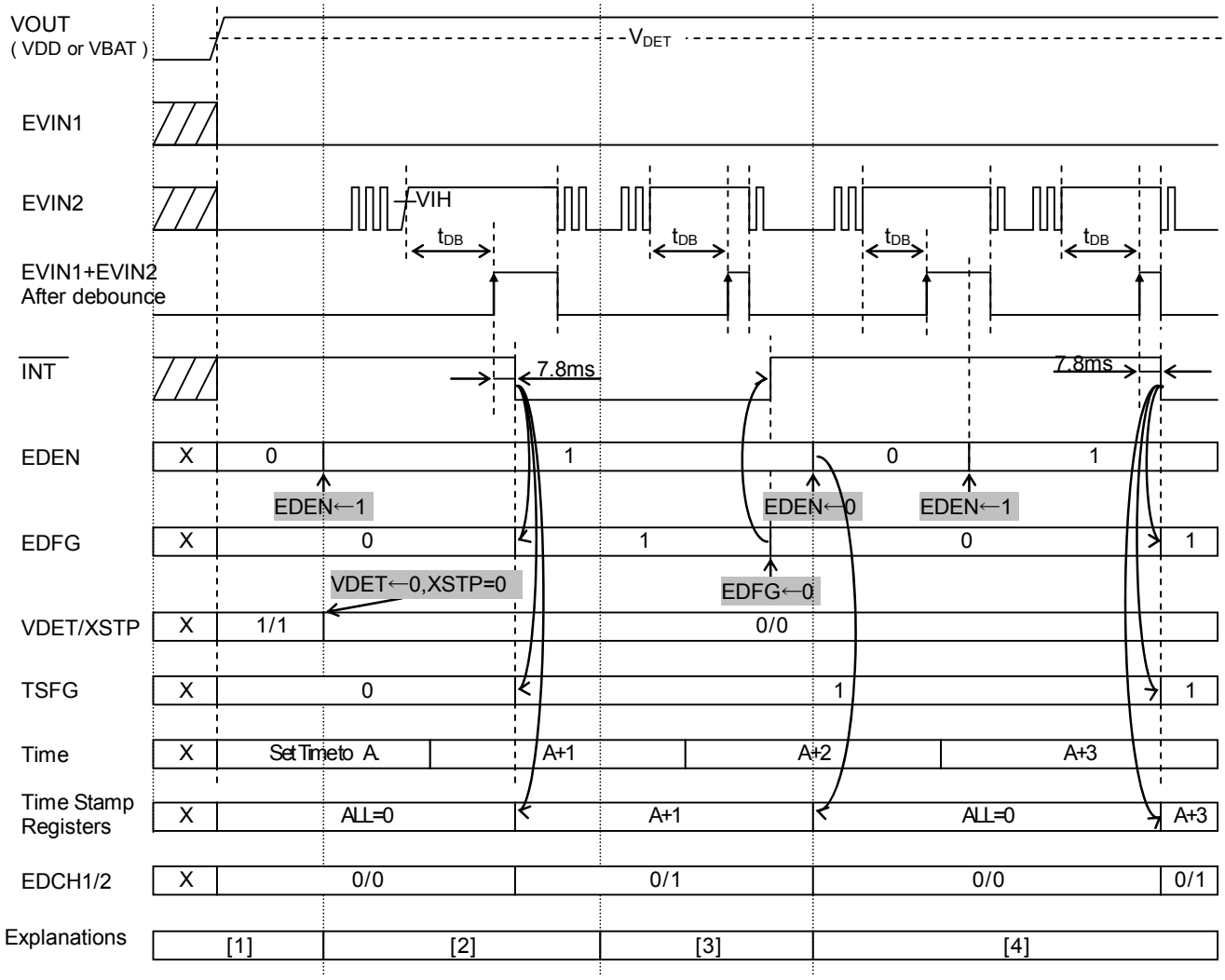
As for the EDFG flag, only clearing to a zero is possible

As for the INT output of event detection, it is assumed that

When EDFG is cleared by zero, INT output is disabled.

Event detection is available in both of VBAT or VDD.

8.4.5 Event detection timing chart.



The operation procedure. Explanation number shows step number in timing chart.

[1]

Set time and date.

please initialize, clear to zero the VDET and XSTP, and set to 1 EDEN.

Set an input terminal of EVIN1,2 in Low level before setting EDEN to 1.

[2]

It is a steady event detection operation.

When event is input into EVIN2 terminal, event is detected tDB time later.

After 7.8ms, ,EDCH2bit is set at 1 to 1 EDFGbit in Low INT.

The time at that time is recorded in Time Stamp Register.

[3]

The condition that was input event into with event detection condition again.

Nothing changes to have already become EDFG=1.

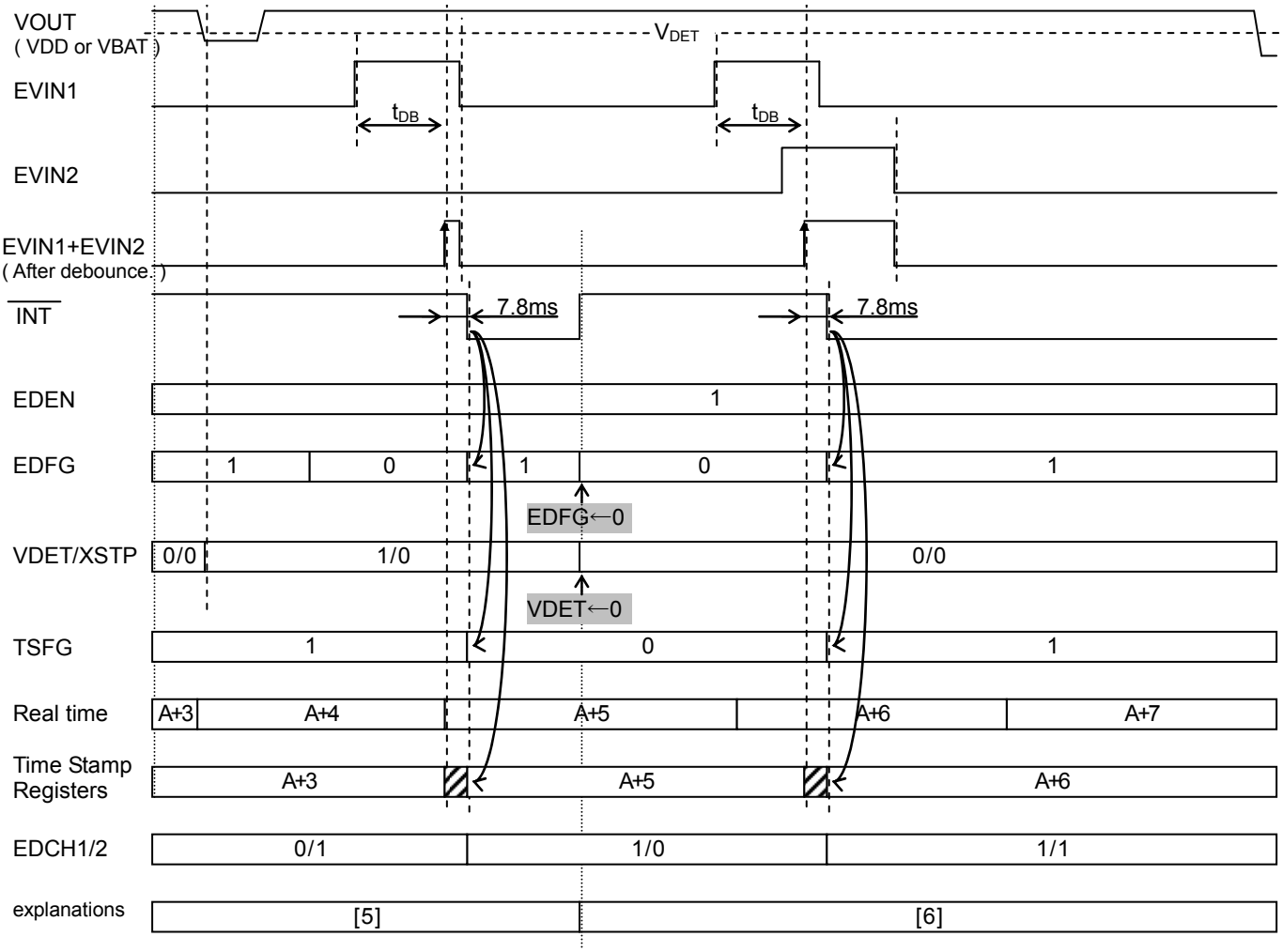
INT terminal is released by Hi-Z when assumed a zero clear EDFG then.

[3]

When EDEN is cleared by a zero, all Time Stamp Register is cleared.

[4]

While event is input, event detection is not performed even if EDEN is set to 1.



[5]
When VOUT voltage dropped in less than VDET voltage, a VDET bit is set to 1.
When event is detected, at the time of VDET=1, TSFG is cleared to 0.
And so TSFG=0 shows that a time stamp is untrustworthy.
Time-Stamp Registers is cleared to zero in hatching period.

[6]
When the EVIN1 and EVIN2 input within tDB, both EDCH1,EDCH2 set to 1.
Time-Stamp Registers is cleared to zero in hatching period.

8.5 Clock Precision Adjustment Function

The clock precision can be set ahead or behind.
This function can be used to implement a higher-precision clock function, such as by:

- enabling higher clock precision throughout the year by taking seasonal clock precision adjustments into account in advance, or
- enabling correction of temperature-related clock precision variation in systems that include a temperature detection function.

∗ Note:
Only the clock precision can be adjusted. The adjustments have no effect on the 32.768kHz output from the FOUT pin.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	Digital Offset (Default)	TEST (0)	F6 (0)	F5 (0)	F4 (0)	F3 (0)	F2 (0)	F1 (0)	F0 (0)

∗) TEST must be cleared surely.

- The binary encoded settings in the seven bits from F6 to F0 are used to set the precision of the clock generated from the 32.768kHz internal oscillator up to $\pm 189.1 \times 10^{-6}$ in the forward (ahead) or reverse (behind) direction, in units of $\pm 3.05 \times 10^{-6}$.

∗1) When not using this function, be sure to set "0" for bits F6 to F0.
∗2) This function operates every twenty seconds (at 00 seconds, 20 seconds, and 40 seconds within each minute), which changes the cycle of the periodic interrupts that occur via this timing.
(See "9.5. Periodic Interrupt Function".)
∗3) Always, clear TEST bits to "0" surely.
Note : TEST can be set to 1 by write access. Be careful.

8.5.1. Adjustment clock precision

1) Adjustment range and resolution

Adjustment range	Adjustment resolution	Internal timing of adjustment
-189.1×10^{-6} to $+189.1 \times 10^{-6}$	$\pm 3.05 \times 10^{-6}$	Once every 20 seconds (at "00", "20" and "40" seconds)

2) Adjustment amount and adjustment value

Adjustment amount ($\times 10^{-6}$)	Adjustment data Decimal / Hexadecimal	bit 7 0	bit 6 F6	bit 5 F5	bit 4 F4	bit 3 F3	bit 2 F2	bit 1 F1	bit 0 F0
−189.10	+63 / 3F h	0	0	1	1	1	1	1	1
−186.05	+62 / 3E h	0	0	1	1	1	1	1	0
−183.00	+61 / 3D h	0	0	1	1	1	1	0	1
⋮	⋮	⋮							
−9.15	+4 / 04	0	0	0	0	0	1	0	0
−6.10	+3 / 03	0	0	0	0	0	0	1	1
−3.05	+2 / 02 h	0	0	0	0	0	0	1	0
OFF	1 / 01 h	0	0	0	0	0	0	0	1
OFF	0 / 00 h	0	0	0	0	0	0	0	0
+3.05	−1 / 7F h	0	1	1	1	1	1	1	1
+6.10	−2 / 7E h	0	1	1	1	1	1	1	0
+9.15	−3 / 7D h	0	1	1	1	1	1	0	1
⋮	⋮	⋮							
+183.00	−60 / 44 h	0	1	0	0	0	1	0	0
+186.05	−61 / 43 h	0	1	0	0	0	0	1	1
+189.10	−62 / 42 h	0	1	0	0	0	0	1	0
OFF	−63 / 41 h	0	1	0	0	0	0	0	1
OFF	−64 / 40 h	0	1	0	0	0	0	0	0

8.5.2 Adjustment examples

Example 1) Setting time forward

Objective) To adjust (advance) the clock precision when FOUT clock output is 32.7677kHz

(1) Determine the current amount of variance

$32.7677\text{kHz} \rightarrow (32.7677 - 32.768) / 32.768$ ∗ [32.768] = Reference values
$\rightarrow -9.16 \times 10^{-6}$

(2) Calculate the optimum adjustment data (decimal value) relative to the current variance.

Adjustment data = variance / adjustment resolution
$= -9.16 / 3.05$
≈ -3 (decimal values are roundeDDown from 4 and up from 5)

∗ For adjusting forward from a retarded variance, this formula can be corrected using reciprocal numbers, but since this product inverts the +/- attributes, this formula can be used as it is.

(3) Calculate the setting adjustment data (hexadecimal)

To calculate the setting adjustment data while taking 7-bit binary encoding into account, subtract the adjustment data (decimal) from 128 (80h).

Setting adjustment data $= 128 - 3 = 125$ (decimal)
$= 80\text{h} - 03\text{h} = 7\text{Dh}$ (hexadecimal)

Example 2) Setting time backward

Objective) To adjust (set back) the clock precision when FOUT clock output is 32.7683kHz

(1) Determine the current amount of variance

$32.7683\text{kHz} \rightarrow (32.7683 - 32.768) / 32.768$ ∗ [32.768] = reference values
$\rightarrow +9.16 \times 10^{-6}$

(2) Calculate the optimum adjustment data (decimal value) relative to the current variance.

Adjustment data = (variance / adjustment resolution) + 1
$= (+9.16 / 3.05) + 1$ ∗ ADD 1 since reference value is 01h
$\approx +4$ (decimal values are roundeDDown from 4 and up from 5)

∗ For adjusting backward from an advanced variance, this formula can be corrected using reciprocal numbers, but since this product inverts the +/- attributes, this formula can be used as it is.

(3) Calculate the setting adjustment data (hexadecimal)

The value "4" can be used in hexadecimal as it is (04h).

Setting adjustment data = 04 h (hexadecimal)

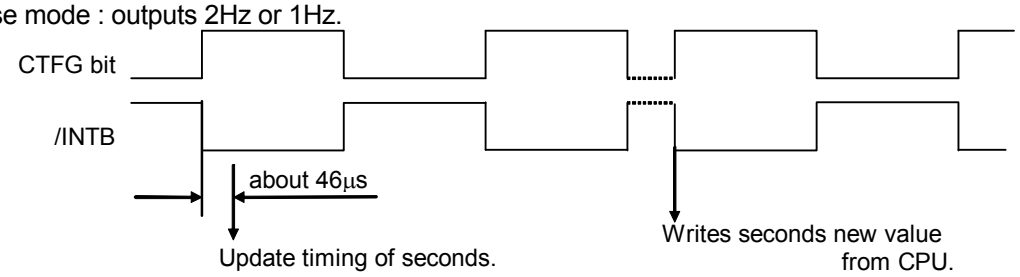
8.6 Periodic Interrupt Function

Periodic interrupt output can be obtained via the INTRB pin.
Select among five periodic-cycle settings: 2 Hz (once per 0.5 seconds), 1 Hz (once per second), 1/60 Hz (once per minute), 1/3600 Hz (once per hour), or monthly (on the 1st of each month).
Select among two output waveforms for periodic interrupts: an ordinary pulse waveform (2 Hz or 1 Hz) or a waveform (every second, minute, hour, or month) for CPU-level interrupts that can support CPU interrupts.
A polling function is also provided to enable monitoring of pin states via registers.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Control 1 (Default)	WkALE (0)	MoALE (0)	DBSL (0)	EDEN (0)	TEST (0)	**CT2 (0)**	**CT1 (0)**	**CT0 (0)**
F	Control 2 (Default)	BANK TSFG (0)	VDET (0)	XSTP (0)	PON (1)	EDFG (0)	CTFG **(0)**	WkAFG (0)	MoAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) " – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

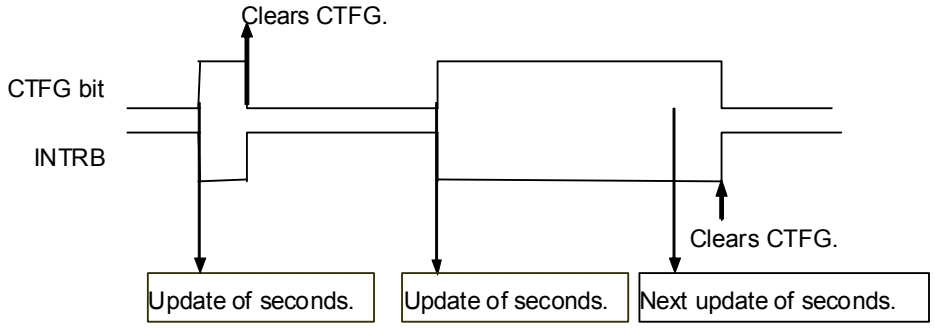
*1)Pulse mode : outputs 2Hz or 1Hz.



In a pulse mode, update of seconds is behind with about 46μs from a falling edge of INTRB.
Therefore, during this 46μs, please consider it because the time and calendar is old.
When CPU writes seconds new value, INTRB outputs low level. Cause is because new value was written to seconds.

*2)Level mode:

A interrupt period selectable from 1s,1min, 1hour and a month.
Count up of a second synchronizes with an falling edge of INTRB.
The timing chart example that an interrupt period set in every seconds.



Note:

When Clock Precision Adjustment Function works, a period of interrupt changes by that quantity of the adjustment once per 20 seconds or one minute.

Pulse mode: ±3.784 msec changes at the maximum for a High section of an output pulse of 1Hz.
And Duty is 50±0.3784%.
±3.784 msec changes at the maximum for a Low section of an output pulse of 2Hz.
And Duty is 50±0.3784%.

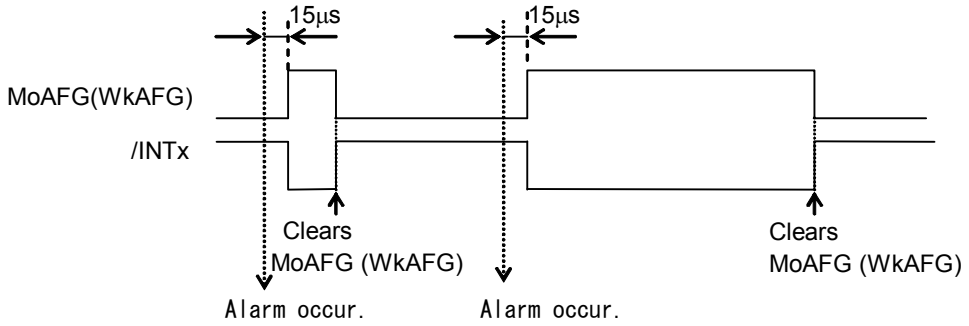
Level mode: Once per second period changes ±3.784ms maximum.

8.7 Alarm Interrupt Function

8.7.1 MoAFG, WkAFG

MoAFG, WkAFG	Status	
0	Alarm does not yet occur.	(Default)
1	Alarm occurred.	

When MoALE or WkALE bits are 1, these flag bits are worked. When alarm occurs, after 61μs these flag bit are set to 1. CPU can clear by 0 , but can not set 1 to these bits.
When MoALE,WkALE is "0", value of MoAFG,WkAFG are "0" always.



8.7.2 Alarm_Wk register (BANK=0 Address 8-Ah)

Alarm_Wk minutes register (BANK=0, address 8h)

D7	D6	D5	D4	D3	D2	D1	D0	
*	WkM40	WkM20	WkM10	WkM8	WkM4	WkM2	WkM1	
0	0	0	0	0	0	0	0	Default

Alarm_Wk Hours register (BANK=0, address 9h)

D7	D6	D5	D4	D3	D2	D1	D0	
*	*	WkH20 WkP/$\overline{A}$	WkH10	WkH 8	WkH4	WkH 2	WkH1	
0	0	0	0	0	0	0	0	Default

Alarm_Wk Weekday register (BANK=0, address Ah)

D7	D6	D5	D4	D3	D2	D1	D0	
*	WkW6	WkW5	WkW4	WkW3	WkAW2	WkW1	WkW0	
0	0	0	0	0	0	0	0	Default

*) Default = When PON bit was set by power-on, default value loads automatically.

- As for the * bit, read and write are possible, like RAM. And the value is not related to alarm.
- When MoALE=0, it can be used as user RAM each Alarm_Wk(3 bytes).
  D5 bit of Alarm_Mo register shows AM,PM in the 12 hours system.(AM=0, PM=1) and shows AH20 (20 digit of hours.)
  Hour counter(Address 02) is update to 32(BCD) from PM11.
- WkW0 to WkW6 is compare the day of week counter. (W4,W2,W1) =(0,0,0) to (1,1,0).
- When AW6 from AW0 are all "0", Alarm_Mo does not works.

8.7.3 Alarm_Mo Register(BANK=0 and 1 (Bh and Ch）

Alarm_Mo minutes register (BANK=0, Address Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
*	MoM40	MoM20	MoM10	MoM8	MoM4	MoM2	MoM1	
0	0	0	0	0	0	0	0	(Default*)

Alarm_Mo Hours register (BANK=0,Address Ch)

D7	D6	D5	D4	D 3	D2	D1	D0	
*	*	MoH20 MoP/ $\overline{A}$	MoH10	MoH8	MoH4	MoH2	MoH1	
0	0	0	0	0	0	0	0	(Default*)

Alarm_Mo Day Register (BANK=1,Address Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
DYE	*	MoD20	MoD10	MoD8	MoD4	MoD2	MoD1	
0	0	0	0	0	0	0	0	(Default*)

Alarm_Mo Month Register (BANK=1, AddressCh)

D7	D6	D5	D4	D3	D2	D1	D0	
MOE	*	*	MoMO10	MoMO8	MoMO4	MoMO2	MoMO1	
0	0	0	0	0	0	0	0	(Default*)

*) Default = When PON bit was set by power-on, default value loads automatically.

- As for the * bit, read and write are possible, like RAM. And the value is not related to alarm.
- When MoALE=0, it can be used as user RAM each Alarm_Mo(4 bytes).
  D5 bit of Alarm_Mo register shows AM,PM in the 12 hours system.(AM=0, PM=1) and shows AH20 (20 digit of hours.)
  Hour counter(Address 02) is update to 32(BCD) from PM11.
- DYE enables day of Alarm_Wk、MOE enables Month of Alarm_Wk。

Usage of DYE, MOE.

MOE	DYE	Alarm occurs. (WoALE = 1 : Enables alarm of week.)	
0	0	Hours and Minutes. (Once per day.)	Default
0	1	Day, Hours and Minutes.(Once per Month.)	
1	0	Month, Hours, and Minutes. (Once per day in selected month.)	
1	1	Month, Days, Hours, and Minutes. (once per year.)	

8.7.4 Programming example of time alarm.

Ex.1) Every year January 3th 9:23.

Registers of Alarm_Wk.		Bit layout.							
		D7	D6	D5	D4	D3	D2	D1	D0
8h in Bank0.	Minutes	0	0	1	0	0	0	1	1
9h in Bank0.	Hours	0	0	0	0	1	0	0	1
Bh in Bank1.	Days	1	0	0	0	0	0	1	1
Ch in Bank1.	Month	1	0	0	0	0	0	0	1

Ex.2)Every month 7th PM 5:13 in 12hour system.

Registers of Alarm_Wk.		Bit layout.							
		D7	D6	D5	D4	D3	D2	D1	D0
8h in Bank0.	Minutes	0	0	0	1	0	0	1	1
9h in Bank0.	Hours	0	0	1	0	0	1	0	1
Bh in Bank1.	Days	1	0	0	0	0	1	1	1
Ch in Bank1.	Month	0	x	x	x	x	x	x	x

Ex.3） Every day 23:45.

Registers of Alarm_Wk.		Bit layout.							
		D7	D6	D5	D4	D3	D2	D1	D0
8h in Bank0.	Minutes	0	1	0	0	0	1	0	1
9h in Bank0.	Hours	0	0	1	0	0	0	1	1
Bh in Bank1.	Days	0	x	x	x	x	x	x	x
Ch in Bank1.	Month	0	x	x	x	x	x	x	x

Note: The value of "x" does not affect Alarm function.

7) WkAFG (MoAFG) bit

These bits are valid only when the WkALE (MoALE) bit value is "1". The WkAFG (MoAFG)bit set to "1" when Alarm Wk (Alarm Mo) has occurred.

The INTRB (INTRA) = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

WkAFG (MoAFG)	Data	Description
Write	0	INTRB (INTRA) pin = OFF = Hi-z ＊Default
	1	Can not write 1.
Read	0	Alarm_Wk (Alarm Mo) time setting does not match current time. ＊Default This bit's value is always "0" when the WkALE (MoALE) bit's setting is "0")
	1	Alarm_Wk occurred. This bit value"1" is kept until cleared to zero.

8.7.5 Alarm_Mo function

The Alarm_Mo function generates interrupt signals (output via the INTRA pin) that correspond to specified month, date, hours and minutes. A polling function is also provided to enable checking of each alarm mode by the host.

Related registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1h inBank0	Minutes	—	M40	M20	M10	M8	M4	M2	M1
2h in Bank0	Hours	—	—	H20 P , /A	H10	H8	H4	H2	H1
4h in Bank0	Day of month	—	—	D20	D10	D8	D4	D2	D1
5h Bank0	Months	—	—	—	MO10	MO8	MO4	MO2	MO1
Bh Bank0	Alarm_Mo ; Minute	*	MoM40	MoM20	MoM10	MoM8	MoM4	MoM2	MoM1
Ch Bank0	Alarm_Mo ; Hour	*	*	MoH20 Mo P/ $\overline{A}$	MoH10	MoH8	MoH4	MoH2	MoH1
Bh Bank1	Alarm_Mo ; Day	DYE	*	MoD20	MoD10	MoD8	MoD4	MoD2	MoD1
Ch Bank1	Alarm_Mo ; Month	MOE	*	*	MoMO10	MoMO8	MoMO4	MoMO2	MoMO1
Eh	Control 1 (Default)	WkALE (0)	MoALE (0)	DBSL (0)	EDEN (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)
Fh	Control 2 (Default)	BANK TSFG (0)	VDET (1)	XSTP (1)	PON (1)	EDFG (0)	CTFG (0)	WkAFG (0)	MoAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.

∗2) " – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

- When the Alarm_Mo setting matches the current time, INTRA pin is set to "L" and the MoALE bit is set to "1".
  Note: If the current date/time is used as the Alarm_Mo setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_Mo ; Hours" register's bit 5 (MoH20, MoP, /A) functions as MoH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.

1) MoALE bit

This bit is used to set up the Alarm_Mo function.

MoALE	Data	Description
Write / Read	0	Alarm_Mo, match comparison operation invalid ∗ Default
	1	Alarm_Mo, match comparison operation valid (INTRA = "L" when match occurs)

∗ When using the Alarm_Mo function, first set this MoALE bit value as "0," then stop the function. Next, set current time and date, and reset the MoAFG bit. Finally, set "1" to the MoALE bit for Alarm_Mo function as valid.

The reason for first setting the MoALE bit value as "0" is to prevent INTRA = "L" output in the event that a match between the current time and alarm setting occurs while the alarm setting is still being made.

2) MoAFG bit

This bit is valid only when the MoALE bit value is "1". When a match occurs between the Alarm_Mo setting and the current time, the MoAFG bit value becomes "1" approximately 61 μs afterward. (There is no effect when the MoALE bit becomes "0".)

The INTRA = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

MoAFG	Data	Description
Write	0	INTRA pin = OFF (Hi-z) (only when the Event detection output is OFF) ∗ Default
	1	Can not write 1.
Read	0	Alarm_Mo time setting does not match current time ∗ Default (This bit's value is always "0" when the MoALE bit's setting is "0")
	1	Alarm_Mo time setting matches current time (result is that bit value is held until cleared to zero)

∗ When a "0" is written to the MoAFG bit, provisionally the MoAFG bit value is "0" and the INTRA pin status is OFF (Hi-z). However, as long as the MoALE bit value is "1" the Alarm_Mo function continues to operate, and Alarm_Mo occurs again the next time the same specified time arrives.

You can stop Alarm_Mo from occurring by writing "0" to the MoALE bit to set this function as invalid.

8.7.6 Alarm_Wk function

The Alarm_Wk function generates interrupt signals (output via the INTRB pin) that correspond to specified days, hours, and minutes. For description of the Alarm Wk function, which supports only hour and minute data, see "8.6. Alarm Wk Function". Multiple day settings can be selected (such as Monday, Wednesday, Friday, Saturday, and Sunday). A polling function is also provided to enable checking of each alarm mode by the host.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	Minutes	—	M40	M20	M10	M8	M4	M2	M1
2	Hours	/12, 24	—	H20 P, /A	H10	H8	H4	H2	H1
3	Days	—	—	—	—	—	W4	W2	W1
8	Alarm_Wk ; Minute	—	WkM40	WkM20	WkM10	WkM8	WkM4	WkM2	WkM1
9	Alarm_Wk ; Hour	—	—	WkH20 WkP, /A	WkH10	WkH8	WkH4	WkH2	WkH1
A	Alarm_Wk ; Day	—	WkW6	WkW5	WkW4	WkW3	WkW2	WkW1	WkW0
E	Control 1 (Default)	WkALE (0)	MoALE (0)	DBSL —	EDEN (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)
F	Control 2 (Default)	BANK TSFG (0)	VDET (0)	XSTP (–)	PON (1)	EDFG (0)	CTFG (0)	WkAFG (0)	MoAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) "○" indicates write-protected bits. A zero is always read from these bits.
∗3) " – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

- When the Alarm_Wk setting matches the current time, INTRB pin is set to "L" and the WkALE bit is set to "1".
  Note: If the current date/time is used as the Alarm_Wk setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_Wk ; Hours" register's bit 5 (WkH20, WkP, /A) functions as WkH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.
- When the Alarm_Wk function's day values (WkW6 to WkW0) are all "0" Alarm_Wk does not occur.

1) WkALE bit
This bit is used to set up the Alarm Wk function to generate alarms matching Weekday, hours and minutes.

WkALE	Data	Description
Write / Read	0	Alarm_Wk, match comparison operation invalid ∗ Default
	1	Alarm_Wk, match comparison operation valid (INTRB = "L" when match occurs)

∗ When using the Alarm Wk function, first set this WkALE bit value as "0," then stop the function. Next, set the weekday, hour, minute, and the WkAFG bit. Finally, set "1" to the WkALE bit to set the Alarm_Wk function as valid. The reason for first setting the WkALE bit value as "0" is to prevent INTRB = "L" output in the event that a match between the current time and alarm setting occurs while the alarm setting is still being made.

2) WkAFG bit
This bit is valid only when the WkALE bit value is "1". When a match occurs between the Alarm_Wk setting and the current time, the WkAFG bit value becomes "1" approximately 61 μs afterward. (There is no effect when the WkALE bit becomes "0".)
The INTRB = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

WkAFG	Data	Description
Write	0	INTRB pin = OFF (Hi-z) ∗ Default
	1	Can not write 1.
Read	0	Alarm_Wk time setting does not match current time ∗ Default (This bit's value is always "0" when the WkALE bit's setting is "0")
	1	Alarm_Wk setting matches current time (Result is that bit value is held until cleared to zero)

When a "0" is written to the WkAFG bit, the INTRB pin status is OFF (Hi-z).
However, as long as the WkALE bit value is "1" the Alarm_Wk function continues to operate, and Alarm_Wk occurs again the next time the same specified time arrives.
You can stop next Alarm_Wk by writing "0" to the WkALE bit.

3) /12, 24 bit

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

/12,24	Data	Description	Address 2 (Hours register) data [h] during 24-hour and 12-hour clock operation modes
Write / Read	0	12-hour clock	
	1	24-hour clock	

24-hour clock	12-hour clock
00	12 (AM 12)
01	01 (AM 01)
02	02 (AM 02)
03	03 (AM 03)
04	04 (AM 04)
05	05 (AM 05)
06	06 (AM 06)
07	07 (AM 07)
08	08 (AM 08)
09	09 (AM 09)
10	10 (AM 10)
11	11 (AM 11)

24-hour clock	12-hour clock
12	32 (PM 12)
13	21 (PM 01)
14	22 (PM 02)
15	23 (PM 03)
16	24 (PM 04)
17	25 (PM 05)
18	26 (PM 06)
19	27 (PM 07)
20	28 (PM 08)
21	29 (PM 09)
22	30 (PM 10)
23	31 (PM 11)

∗ Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

4) Day setting

The following table shows the correspondence between the current day (W4, W2, W1) and the Alarm_Wk day (WkW6 to WkW0). Be sure to set a "1" to the Alarm_Wk day when the alarm will occur. (An alarm will not occur for any day that has a "0" setting.)

It is possible to enter settings for several days at the same time, in which case be sure to set a "1" for each day (among WkW6 to WkW0) in which an alarm will occur.

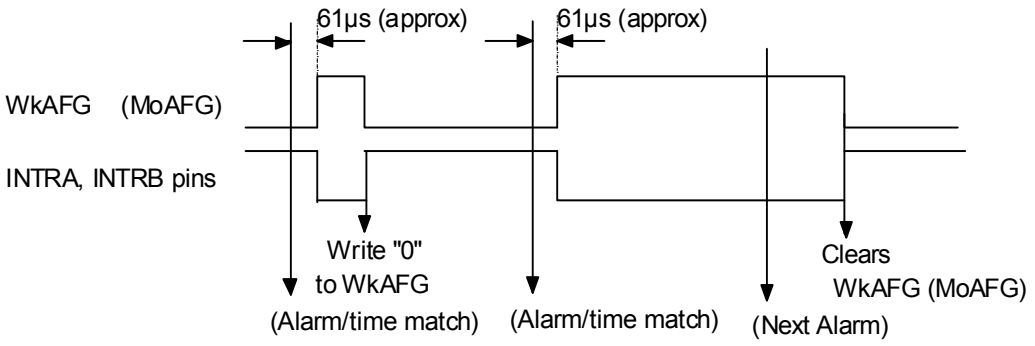
Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Alarm_Wk ; Day	□	WkW6	WkW5	WkW4	WkW3	WkW2	WkW1	WkW0
Target day(s) (W4,W2,W1)	–	Saturday (1, 1, 0)	Friday (1, 0, 1)	Thursday (1, 0, 0)	Wednesday (0, 1, 1)	Tuesday (0, 1, 0)	Monday (0, 0, 1)	Sunday (0, 0, 0)

8.7.7 Alarm setting examples

Examples of settings for alarm usage are shown below.

Alarm needs (example)		Alarm_Wk ; Day Day setting							Alarm_Wk ; Hour Hour (hexadecimal)		Alarm_Wk ; Minute Minute (hexadecimal)
		WkW6 Sat	WkW5 Fri	WkW4 Thu	WkW3 Wed	WkW2 Tue	WkW1 Mon	WkW0 Sun	24-hour clock	12-hour clock	12- & 24-hour clock
Every day	at 00:00 AM	1	1	1	1	1	1	1	00h hours	12h hours	00h min
Every day	at 01:30 AM	1	1	1	1	1	1	1	01h hours	01h hours	30h min
Every day	at 11:59 AM	1	1	1	1	1	1	1	11h hours	11h hours	59h min
Mon to Fri	at 12:00 PM	0	1	1	1	1	1	0	12h hours	32h hours	00h min
Sunday	at 01:30 PM	0	0	0	0	0	0	1	13h hours	21h hours	30h min
Mon/Wed/Fri	at 11:59 PM	0	1	0	1	0	1	0	23h hours	31h hours	59h min

8.7.8 (WkAFG, MoAFG) and (INTRA, INTRB) output.



8.8. The various detection Functions

The detection functions include detection of power-on resets, oscillation stops, and supply voltage drops, as well as reporting of detection results in corresponding bits of the address Fh (Control 2) register.
The status of the power supply, oscillation circuit, and clock can be confirmed by checking these results.

∗ Note with caution that detection functions may not operate correctly when power flickers occur.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control 2	**BANK TSFG**	**VDET**	**XSTP**	**PON**	**EDFG**	**CTFG**	**WkAFG**	**MoAFG**
	(Default)	**(0)**	**(1)**	**(1)**	**(1)**	(0)	(0)	(0)	(0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.

8.8.1. Power-on reset detection

This function detects when a power-on reset occurs. When a power-on reset is detected, the PON bit value becomes "1". A reset is detected when a power-on from 0 V has occurred, including when the power-on reset from 0 V occurred due to a supply voltage drop.

1) PON bit
This bit indicates the detection results when a power-on reset has occurred.
The power-on reset function operates when a power-on from 0 V has occurred, including when a power-on reset from 0 V occurred due to a supply voltage drop. When this function operates, the PON bit value becomes "1".
The XSTP and VDET bits can be used in combination to determine the valid/invalid status of the clock and calendar data.

PON	Data	Description
Write	0	Clears PON bit to zero and sets up for next detection operation
	1	Can not write 1.
Read	0	Power-on reset was not detected
	1	Power-on reset was detected ∗ Default (result is that bit value is held until cleared to zero)

∗ When PON = "1", all bits in the Alarm_Wk, Alarm_Mo, RAM, Digital Offset, Control 1 and Control 2 registers except for the PON and XSTP bits are reset to "0".
This stops (sets Hi-Z for) output from the INTRA and INTRB pins.

2) Status of other bits when power-on reset is detected

- Internal initialization status during a power-on reset

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	Digital Offset	TEST	F6	F5	F4	F3	F2	F1	F0
	(Default)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
E	Control 1	WkALE	MoALE	DBSL	EDEN	TEST	CT2	CT1	CT0
	(Default)	(0)	(0)	(–)	(0)	(0)	(0)	(0)	(0)
F	Control 2	BANK TSFG	VDLOW	XSTP	PON	EDFG	CTFG	WkAFG	MoAFG
	(Default)	(0)	(1)	(1)	(1)	(0)	(0)	(0)	(0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.

∗2) " – " are read-only bits. The read value of these bits are always "0". Writing is null and void.

∗3) At this point, all other register bits are undefined, so be sure to perform a reset before using the module.
Also, be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the time data is incorrect.

8.8.2. Oscillation stop detection

This function detects when internal oscillation has stopped. When an oscillation stop is detected, the XSTP bit value becomes "0".
If a "1" has already been written to the XSTP bit, the XSTP bit is cleared to zero when stopping of internal oscillation is detected, so this function can be used to determine whether or not an oscillation stop has occurred previously, such as after recovery from a backup.

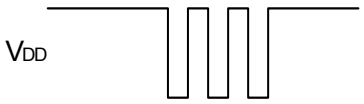
1) XSTP bit
This bit indicates the oscillation stop detection function's detection results.

XSTP	Data	Description
Write	1	Setting prohibited (do not set this bit value, even though it has no effect)
	0	Can not write 1.
Read	1	Oscillation stop was detected (result is that bit value is held until a "1" is written)
	0	Oscillation stop was not detected. The logic of this bit is reverse of RX-8025.

2) Notes

For a normal operation of an oscillation stop detection function, the input of a signal beyond rating and a momentary blackout must not be given.
Please restrain fluctuation of a power supply as shown in a figure when a battery is used.
After big supply fluctuation occurs, maybe internal data are broken, and the XSTP bit value does not changes from "0".
so be sure to avoid input of big chattering.
The logic of this bit is reverse of RX-8025.

Example of voltage fluctuation that makes oscillation stop hard to detect



8.8.3. Battery voltage drop detection

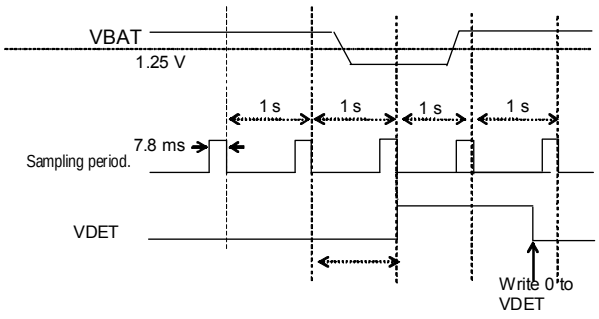
This function detects BAT terminal voltage drop. Detection of a voltage drop sets the VDET bit to "1".

1) VDET bit

VDET	Data	Description
Write	0	Restarts the VBAT drop detection operation and sets up for next VBAT drop detection operation
	1	Can not write 1.
Read	0	VBAT drop was not detected
	1	VBAT drop was detected. ＊Default This drop etection result is maintained till VDET is cleared.

3) Note

To reduce current consumption while monitoring the supply voltage, the supply voltage monitor circuit samples for only 7.8 ms during each second, as shown at right. Sampling is stopped once the VDET bit = "1". (Clear the VDET bit to zero to resume operation of the detection function.)

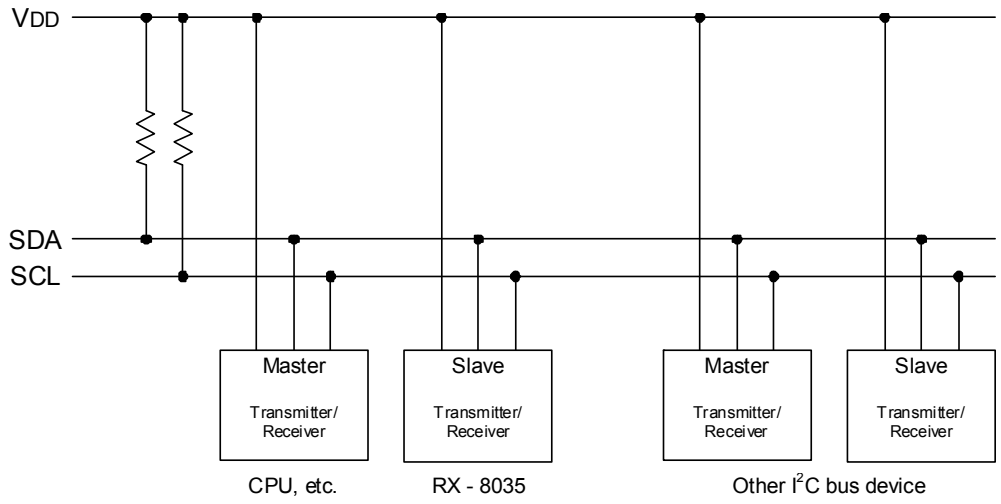


8.9 Overview of I2C-BUS

The I^2C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.
Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.
During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I^2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

8.9.1. System configuration

All ports connected to the I^2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the V_{DD} line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

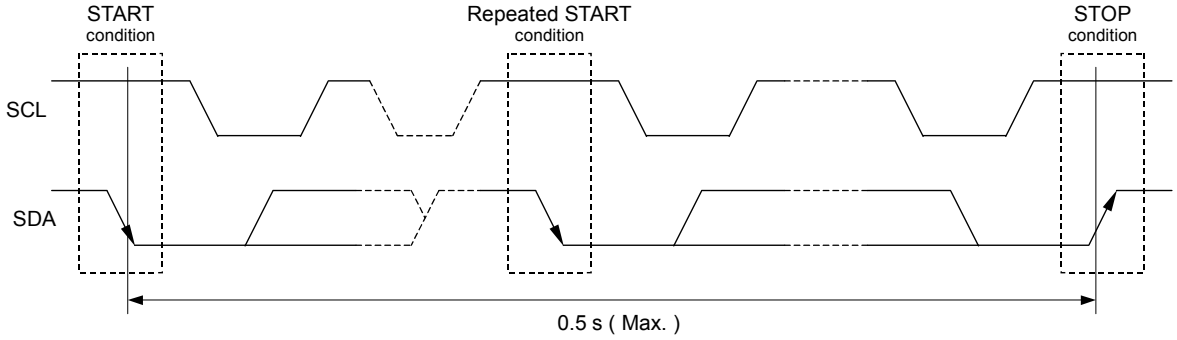


Any device that controls the transmission and reception of data is defined as a master device and any device that is controlled by a master device is defined as a slave device.
Also, any device that transmits data is defined as a transmitter and any device that receives data is defined as a receiver.

In the case of RX-8035, controllers such as a CPU are defined as master devices and the RX-8035 is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

Note
When a crystal oscillation is stopping, RX-8035 cannot output ACK signal in I2C access.
Therefore, In initial-power-ON, please access RX-8035, after crystal oscillation started.
Internal crystal start-up time are 300ms. (Typ.)

8.9.2. Starting and stopping I2C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition

- This condition regulates how communications on the I^2C-BUS are started. SDA level changes from high to low while SCL is at high level

(2) STOP condition

- This condition regulates how communications on the I^2C-BUS are terminated. SDA level changes from low to high while SCL is at high level

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

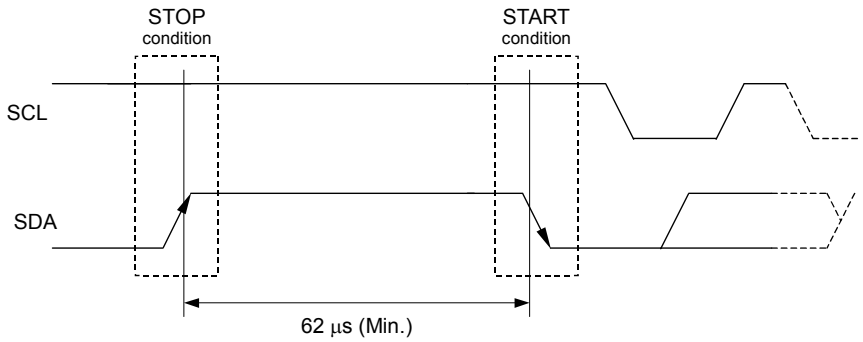
∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RX-8035 is in receiver mode (data reception mode = SDA released).

∗3) When communicating with RX-8035, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within 0.5 seconds. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur within 0.5 seconds.)

If this series of operations requires 0.5 to 1.0 seconds or longer, the I^2C bus interface will be automatically cleared and set to standby mode by RX-8035 bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1").

Restarting of communications begins with transfer of the START condition again.

∗4) When communicating with RX-8035, wait at least 62 µs between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications). (If any carries occur in the time data during this communication period, corrections are made during this period.)



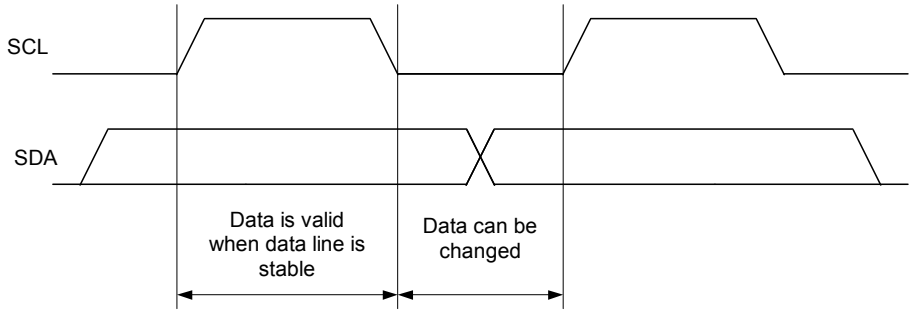
8.9.3. Data transfers and acknowledge responses during I2C-BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.5 seconds and access to the address Dh (Reserved) register is prohibited.)

The address auto increment function operates during both write and read operations.
After address Fh, incrementation goes to address 0h.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.

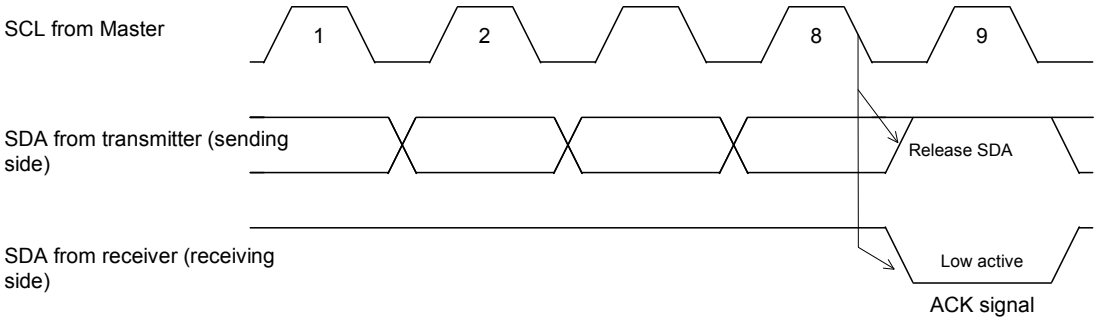


∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

8.9.4. Slave address

The I^2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. RX-8035 slave address is [0110 010∗].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	65 h	0	1	1	0	0	1	0	1 (= Read)
Write	64 h								0 (= Write)

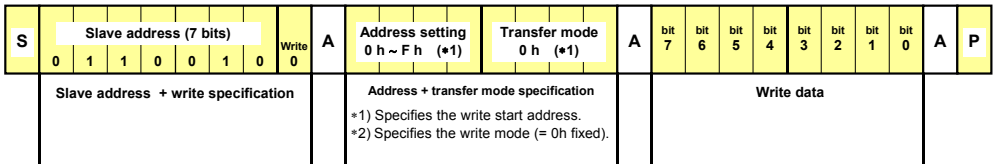
8.9.5. I2C bus's basic transfer format

- The write/read steps are illustrated below.

	Master is transmitter (sending side), RTC is receiver (receiving side)	S	START condition, sent by Master	A	Confirmation response from Master
	Master is receiver (receiving side), RTC is transmitter (sending side)	Sr	RESTART condition, sent by Master	/A	Master does not respond
		P	STOP condition, sent by Master	A	Confirmation response from RTC

1) Write via I^2C bus

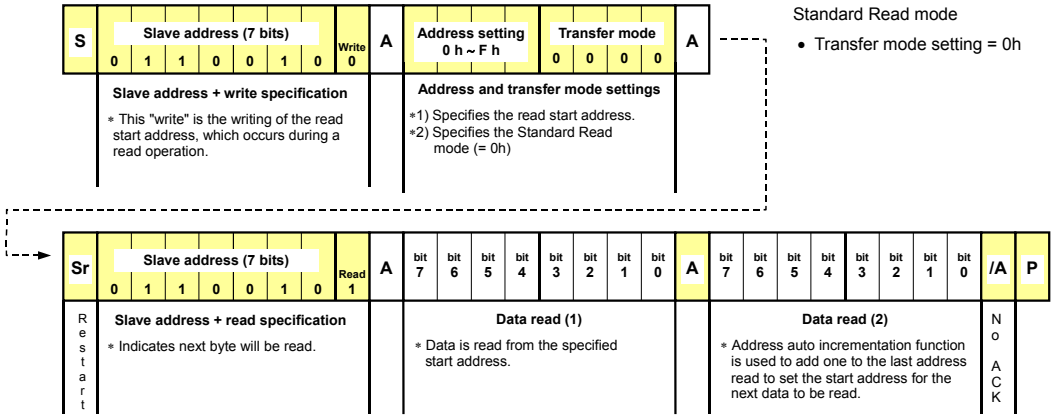
- The steps for writing via the I^2C bus are shown below.



2) Read via I^2C bus

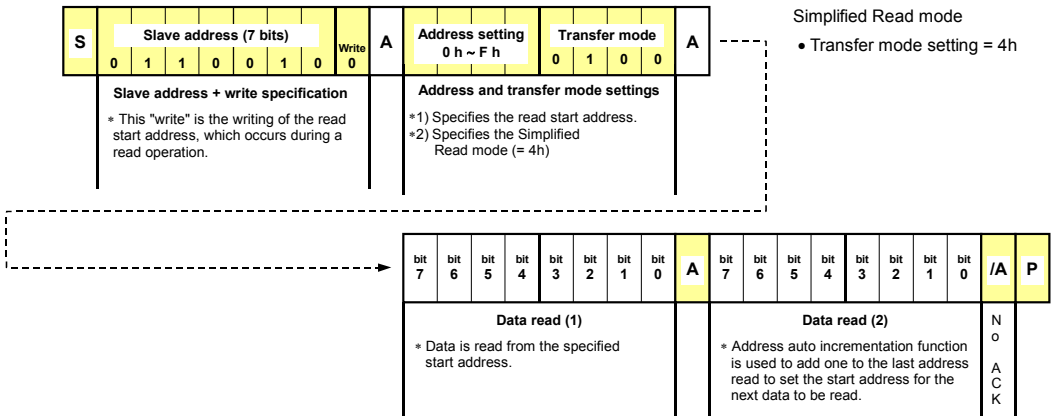
(1) Standard read method for I^2C bus

- The steps for standard reading of the I^2C bus are shown below.



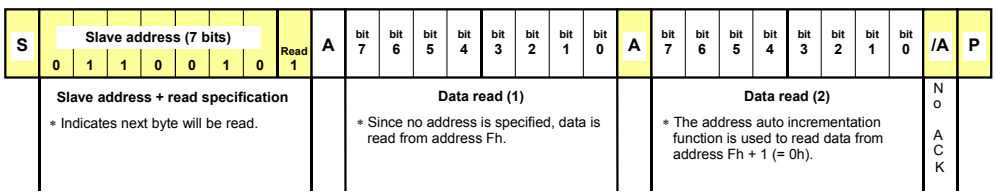
(2) Simplified read method

- RX-8035 also provides a special read method that uses fewer read steps.



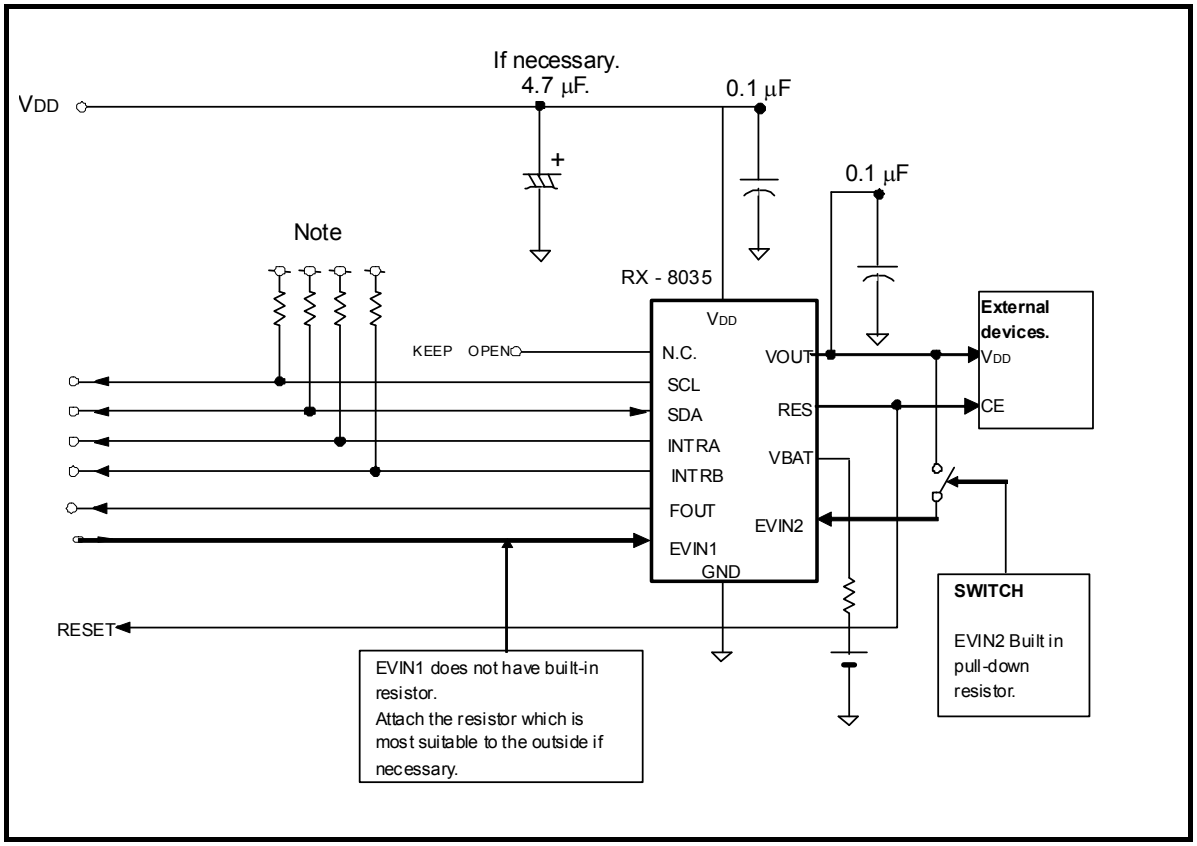
(3) Read method from address Fh, with no specified start address for read operation

- Only when reading from address Fh (Fh → 0h → 1h → 2h, etc.) can a read operation be performed without specifying the read start address or the transfer mode.



* The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications. (However, the transfer time must be no longer than 0.5 seconds and access to the address Dh (Reserved) register is prohibited.)

9. External Connection Example



Note : Pull-up resistor connections.

- SCL and SDA

Connect to the system-power-supply .

- INTRA , INTRB

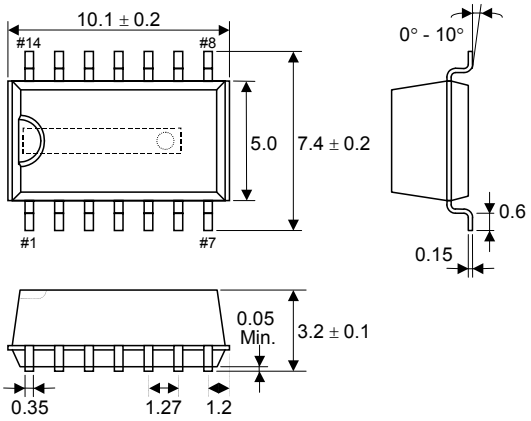
When , uses these interrupt signals at battery backup,
connect these pins to VOUT terminal.(10mA Max.)

10. External Dimensions / Marking Layout

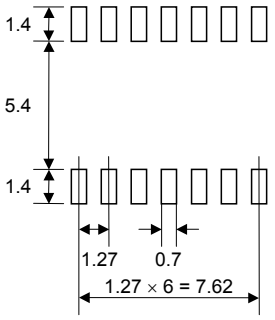
10.1. External Dimensions

RX-8035 SA (SOP-14pin)

• External dimensions



• Recommended soldering

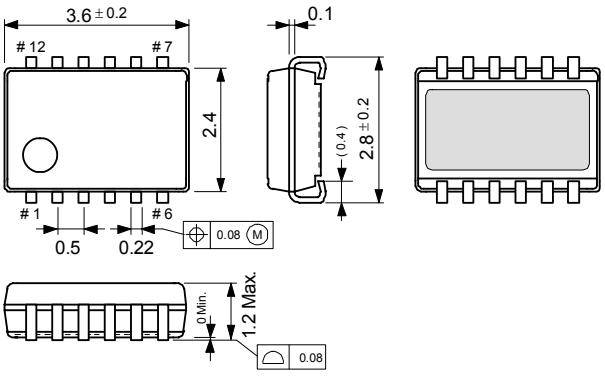


Unit : mm

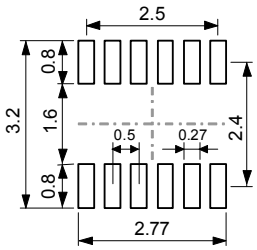
∗ The cylinder of the crystal oscillator can be seen in this area (back and front), but it has no affect on the performance of the device.

RX-8035 LC (VSOJ-12pin)

• External dimensions



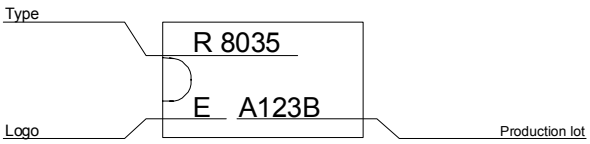
• Recommended soldering



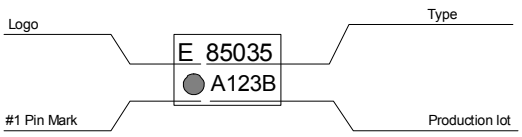
Unit : mm

10.2. Marking Layout

RX - 8035 SA (SOP-14pin)



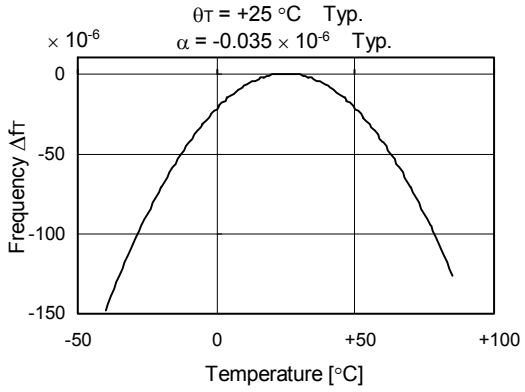
RX – 8035 LC (VSOJ – 12pin)



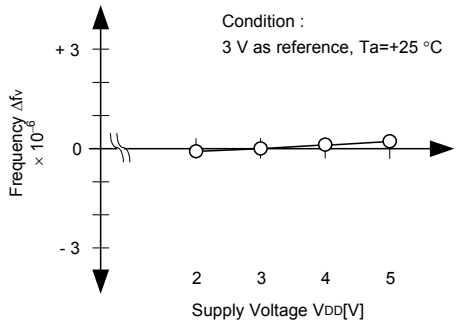
∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

11. Reference Data

(1) Example of frequency and temperature characteristics



(2) Example of frequency and voltage characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha\ (\theta_T - \theta_X)^2$

Δf_T		: Frequency deviation in any temperature
α	(1 / °C^2)	: Coefficient of secondary temperature $(-0.035 \pm 0.005) \times 10^{-6}$ / °C^2
θ_T	(°C)	: Ultimate temperature (+25±5 °C)
θ_X	(°C)	: Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	: Frequency precision
Δf_T	: Frequency deviation in any temperature
Δf_V	: Frequency deviation in any voltage

3. How to find the date difference

Date difference = $\Delta f/f \times 86400$ (seconds)

* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

12. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between V_{DD} and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to V_{DD} or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Packaging equipment

This product uses a molded package whose back contains glass.
Therefore, it is possible for shocks during packaging to cause product breakage, depending on the packaging machinery and conditions.
Please be sure to check that the load placed on products during packaging is as low as possible (low speeds during loading onto the substrate, low chuck forces, etc.) before using packaging equipment.
Carry out the same checks when changing packaging conditions.
The presence of foreign objects between this product and the packaging substrate may result in product breakage.
Guard against introduction of foreign objects during packaging.
Also, carry out measures to eliminate static electricity during packaging of and operations with this product.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

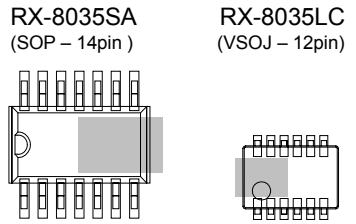
(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

(6) Stop using the glue

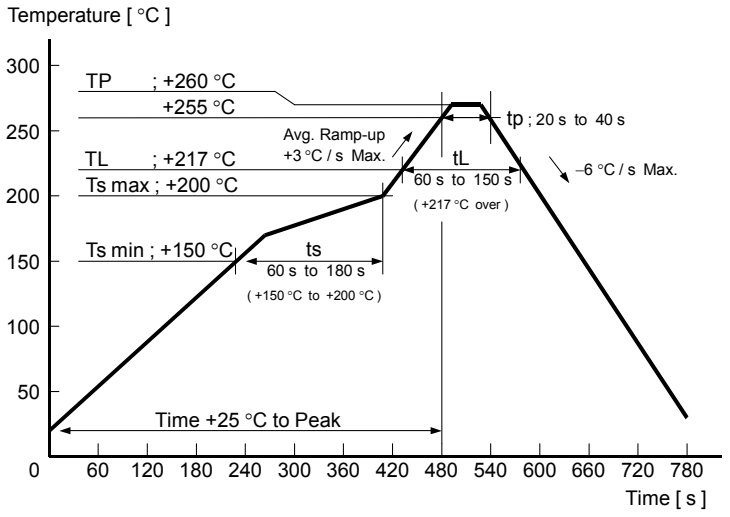
Any glue must never use it after soldering RTC to a circuit board.
This product has glass on the back side of a package.
When glue invasions between circuit board side and glass side, then glass cracks by thermal expansion of glue.
In this case a crystal oscillation stops.
Consider glue abolition or glue do not touch to RTC.

Fig. 1 : Example GND Pattern



∗ The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



Application Manual

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